TRS-80®
MODEL 4/4P
TECHNICAL
REFERENCE
MANUAL

CAT. NO. 26-2119

10 9 8 7 6 5 4 3 2 1

SECTION I

4 THEORY OF OPERATION

Part 1 / Hardware

1.1 MODEL 4 THEORY OF OPERATION

1.1.1 Introduction

The TRS 80 Model 4 Microcomputer is a self contained desktop microcomputer designed not only to be completely software compatible with the TRS 80 Model III, but to pro vide many enhancements and features System distinctions which enable the Model 4 to be Model III compatible include a Z80 CPU capable of running at a 4 MHz clock rate, BASIC operating system in ROM (14K), memory mapped keyboard, 64 character by 16 line memory mapped video display, up to 128K Random Access Memory, cassette circuitry able to operate at 500 or 1500 baud, and the ability to accept a variety of options These options include one to four 5 1/4 inch double density floppy disk drives, one to four five megabyte hard disk drives, an RS 232 Serial Communications Interface, and a 640 by 240 pixel high resolution graphics board

1.1.2 CPU and Timing

The central processing unit of the Model 4 microcomputer is the Z80 A microprocessor – capable of running at either a two (2 02752) or four (4 05504) MHz clock rate The main CPU timing comes from the 20 MHz (20 2752 MHz) crystal controlled oscillator, Y1 and Q1 There is an additional 12 MHz (12 672 MHz) oscillator, Y2 and Q2, which is necessary for the 80 by 24 mode of video operation The oscillator outputs are sent to two Programmable Array Logic (PAL) circuits, U3 and U4, for frequency division and routing of appropriate timing signals

PAL U3 divides the 20 MHz signal by five for 4 MHz CPU operation, by ten for a 2 MHz rate, and slows the 4 MHz clock for the M1 Cycle (See Figure 1-3) U3 also divides the master clock by four to obtain a 5 MHz clock to be sent to the RS-232 option connector as a reference for the baud rate generator PAL U4 selects an appropriate 10 MHz or 12 MHz clock for the video shift clock, and using divider U5 provides additional timing signals to the video display circuitry (See Fig 1-4)

Hex latch U18 is clocked from the 20 MHz clock, and is used to provide MUX and CAS timing for the dynamic memory circuits Also, with additional gates from U16, U19, U20, U31, and U32, this chip provides the wait cir cuitry necessary to prevent the CPU from accessing video RAM during the active portion of the display This is done by latching the data for the video RAM and simultaneously forcing the Z80 CPU into a "WAIT" state and is necessary to eliminate undesirable "hashing" of the video display (See Fig 1-4)

1.1.3 Buffering

Low level signals from and to the CPU need to be buffered, or current amplified in order to drive many other circuits The 16 address lines are buffered by U55 and U56, which are unidirectional buffers that are permanently enabled The eight data lines are buffered by U71 Since data must flow both to and from the CPU, U71 is a bi directional buffer which can go into a three state condition when not in use Both direction and enable controls come from the address decoding section

The clock signal to the CPU (from PAL U3) is buffered by active pullup circuit Q3 RESET and WAIT inputs to the CPU are buffered by U17 and U46 Control outputs from the Z80 (M1*, RD*, WR*, MREQ*, and IORQ*) are sent to PAL U58, which combines these into other appropriate control signals consistent with Model 4's architecture Other than MREQ*, which is buffered by part of U38, the raw control signals go to no other components, and hence require no additional buffering

1.1.4 Address Decoding

The address decoding section is divided into two sub sections Port address decoding and Memory address decoding

In port address decoding, low order address lines (some combined through a portion of U32) are sent to the address and enable inputs of U48, U49, and U50 U48 is also enabled by the IN* signal, which means that is decodes port input signals, while U49 decodes port output signals A table of the resulting port map is shown below

Port Addr. (Hex)	Read Function	Write Function
FC FF	Cassette In, Mode Read	Cassette Out, resets cassette data latch
F8 FB	Read Printer Status	Output to Printer
(1) F4 F7	reserved	Drive Select latch
(1) F3	FDC Data Reg	FDC Data Reg
(1) F2	FDC Sector Reg	FDC Sector Reg
(1) F1	FDC Track Reg	FDC Track Reg.

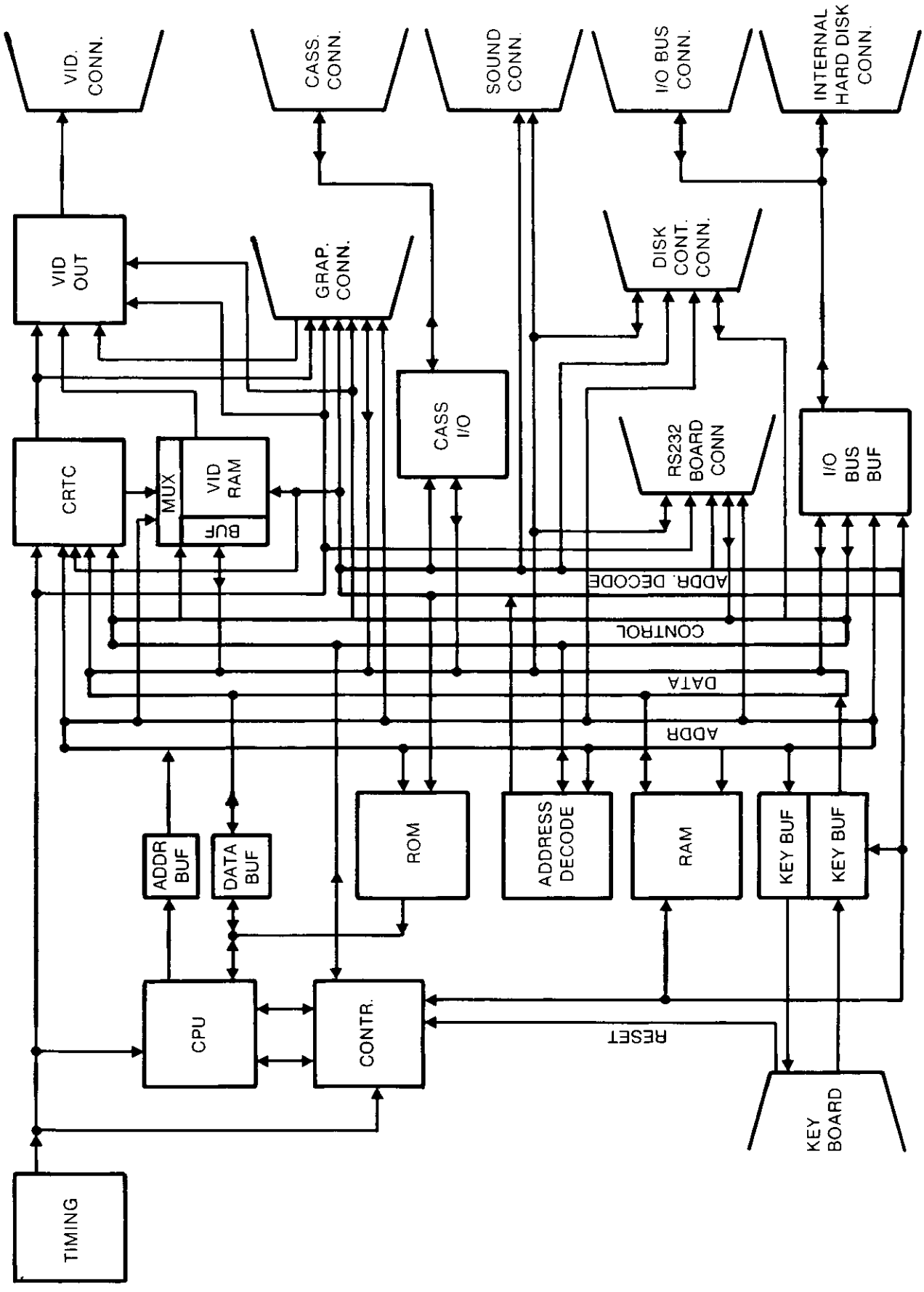


FIGURE 1-1. MODEL 4 BLOCK DIAGRAM

(1)	F0	FDC Status Reg.	FDC Command Reg.
	EC - EF	Resets RTC Int.	Mode Output latch
(2)	EB	Rcvr Holding Reg.	Xmit Holding Reg.
(2)	EA	UART Status Reg.	UART/Modem control
(2)	E9	- reserved -	Baud Rate Register
(2)	E8	Modem Status	Master Reset/Enable UART control reg.
	E4 - E7	Read NMI Status	Write NMI Mask reg.
	E0 - E3	Read INT Status	Write INT Mask reg.
(3)	CF	HD Status	HD Command
(3)	CE	HD Size/Drv/Hd	HD Size/Drv/Hd
(3)	CD	HD Cylinder high	HD Cylinder high
(3)	CC	HD Cylinder low	HD Cylinder low
(3)	CB	HD Sector Number	HD Sector Number
(3)	CA	HD Sector Count	HD Sector Count
(3)	C9	HD Error Reg.	HD Write Precomp.
(3)	C8	HD Data Reg.	HD Data Reg.
(3)	C7	HD CTC channel 3	HD CTC channel 3
(3)	C6	HD CTC channel 2	HD CTC channel 2
(3)	C5	HD CTC channel 1	HD CTC channel 1
(3)	C4	HD CTC channel 0	HD CTC channel 0
(3)	C2 - C3	HD Device ID Reg.	- reserved -
(3)	C1	HD Control Reg.	HD Control Reg.
(3)	C0	HD Wr. Prot. Reg.	- reserved -
	94 - 9F	- reserved -	- reserved -
(4)	90 - 93	- reserved -	Sound Option
(5)	8C - 8F	Graphics Sel. 2	Graphics Sel. 2
	8B	CRTC Data Reg.	CRTC Data Reg.
	8A	CRTC Control Reg.	CRTC Control Reg.
	89	CRTC Data Reg.	CRTC Data Reg.
	88	CRTC Control Reg.	CRTC Control Reg.
	84 - 87	- reserved -	Options Register
(5)	83	- reserved -	Gra. X Reg. Write
(5)	82	- reserved -	Gra. Y Reg. Write
(5)	81	Graphics Ram Rd.	Graphics Ram Wr.
(5)	80	- reserved -	Gra. Options Reg. Wr

Notes:
(1) Valid only if FDC option is installed
(2) Valid only if RS-232 option is installed
(3) Valid only if Hard Disk option is installed
(4) Valid only if sound option is installed
(5) Valid only if High Resolution Graphics option is installed

Following is a Bit Map of the appropriate ports in the Model 4. Note that this is an "internal" bit map only. For bit maps of the optional devices, refer to the appropriate section of the desired manual.

Model 4 Port Bit Map

Port	D7	D6	D5	D4	D3	D2	D1	D0
FC - FF	Cass							Cassette
(READ)	data 500 bd			(MIRROR of PORT EC)				data 1500 bd
FC - FF			(Note, also resets cassette data latch)				cass.	cassette
(WRITE)	x	x	x	x	x	x	out	data out
F8 - FB (READ)	Prntr BUSY	Prntr Paper	Prntr Select	Prntr Fault	x x	x x	x x	x x
F8 - FB (WRITE)	Prntr D7	Prntr D6	Prntr D5	Prntr D4	Prntr D3	Prntr D2	Prntr D1	Prntr D0
EC - EF			(Any Read causes reset of Real Time Clock Interrupt)					
EC - EF (WRITE)	x x	CPU Fast	x x	Enable EX I/O	Enable Altset	Mode Select	Cass Mot On	x x
E0 - E3 (READ)	x x	Receive Error	Receive Data	Xmit Empty	10 Bus Int	RTC Int	C Fall Int	C Rise Int
E0 - E3 (WRITE)	x x	Enable Rec Err	Enable Rec Data	Enable Xmit Emp	Enable 10 Int	Enable RT Int	Enable CF Int	Enable CR Int
90 - 93 (WRITE)	x x	x x	x x	x x	x x	x x	x x	Sound Bit
84 - 87 (WRITE)	Page	Fix Upr Memory	Memory Bit 1	Memory Bit 0	Invert Video	80/64	Select Bit 1	Select Bit 0

Memory mapping is accomplished by PAL U59 in the Basic 16K or 64K computer. In a 128K system, PAL U72, along with the select and memory bits of the options register, also enter into the memory mapping function.

Four memory maps are listed below. Memory Map I is compatible with the Model III. Note that there are two 32K banks in the 64K system, which can be interchanged with either position of the upper two banks of a 128K system. The 128K system has four moveable 32K banks. Also note, in the Model III mode, that decoding for the printer status read (37E8 and 37E9 hexadecimal) is accomplished by U93 and leftover gates from U40, U46, U51, U54, U60, and U62.

Memory Map I — Model III Mode

	0000 – 1FFF	ROM A (8K)
	2000 – 2FFF	ROM B (4K)
	3000 – 37FF	ROM C (2K) – Less 37E8 - 37E9
	37E8 – 37E9	Printer Status Port
	3800 – 3BFF	Keyboard
	3C00 – 3FFF	Video RAM (Page bit selects 1K of 2K)
*	4000 – 7FFF	RAM (16K system)
*	4000 – FFFF	RAM (64K system)

Memory Map II

0000 – 37FF	RAM (14K)	
3800 – 3BFF	Keyboard	
3C00 – 3FFF	Video RAM	
4000 – 7FFF	RAM (16K)	End of one 32K Bank
8000 – FFFF	RAM (32K)	Second 32K Bank

Memory Map III

0000 – 7FFF	RAM (32K)	End of One 32K Bank
8000 – F3FF	RAM (29K)	Second 32K Bank
F400 – F7FF	Keyboard	
F800 – FFFF	Video RAM	

Memory Map IV

0000 – 7FFF	RAM (32K)	One 32K Bank
8000 – FFFF	RAM (32K)	Second 32K Bank

(See Figure 1-2 for 128K Maps)

1.1.5 ROM

The Model 4 Microcomputer contains 14K of Read Only Memory (ROM), which is divided into an 8K ROM (U68), a 4K ROM (U69), and a 2K ROM (U70). ROMs used have three-state outputs which are disabled if the ROMs are deselected. As a result, ROM data outputs are connected directly to the CPU data bus and do not use data buffer U71, which is disabled during a ROM access.

ROMs are Model III compatible and contain a BASIC operating system, as well as a floppy disk boot routine. The enable inputs to the ROMs are provided by the address decoding section, and are present only in the Model III mode of operation.

1.1.6 RAM

Three configurations of Random Access Memory are available on the Model 4: 16K, 64K, and 128K. The 16K option uses 4116 type, 16K by 1 dynamic RAMs, which require three supply voltages (+12 volts, +5 volts, and –5 volts). The 64K and 128K options use 6665 type, 64K by 1 dynamic RAMs, which require only a single supply voltage (+5 volts). The proper voltage for each option is provided by jumpers.

Dynamic RAMs require multiplexed incoming address lines. This is accomplished by ICs U63 and U76. Output data from RAMs is buffered by U64. With the 128K option, there are two rows of the 64K by 1 RAM ICs. The proper row is selected by the CAS* signal from PAL U72.

1.1.7 Keyboard

The Model 4 Keyboard is a 70-key sculptured keyboard, scanned by the microprocessor. Each key is identified by its column and row position. Columns are defined by address lines A0 - A7, which are buffered by open-collector drivers U29 and U30. Data lines D0 - D7 define the rows and are buffered by CMOS buffers U44 and U45. Row inputs to the buffers are pulled up by resistor pack RP 1, unless a key in the current column being scanned is depressed. Then, the row for that key goes low.

1.1.8 Video

The heart of the video display circuitry in the Model 4 is the 68045 Cathode Ray Tube Controller. The CRTC allows two screen formats: 64 by 16 and 80 by 24. Since the 80 by 24 screen requires 1,920 screen memory locations, a 2K by 8 static RAM is used for the Video RAM. The 64 by 16 mode has a two-page screen display and a bit in the options register for determining which page is active for the CPU. Offset the start address of the CRTC to gain access to the second page in the 64 by 16 mode.

Addresses to the video RAM are provided by the 68045 when refreshing the screen and by the CPU when updating the data. These two sets of addresses are multiplexed by U33, U34, and U35. Data between the CPU and Video RAM is latched by U6 for a write, and buffered by U7 for a read operation.

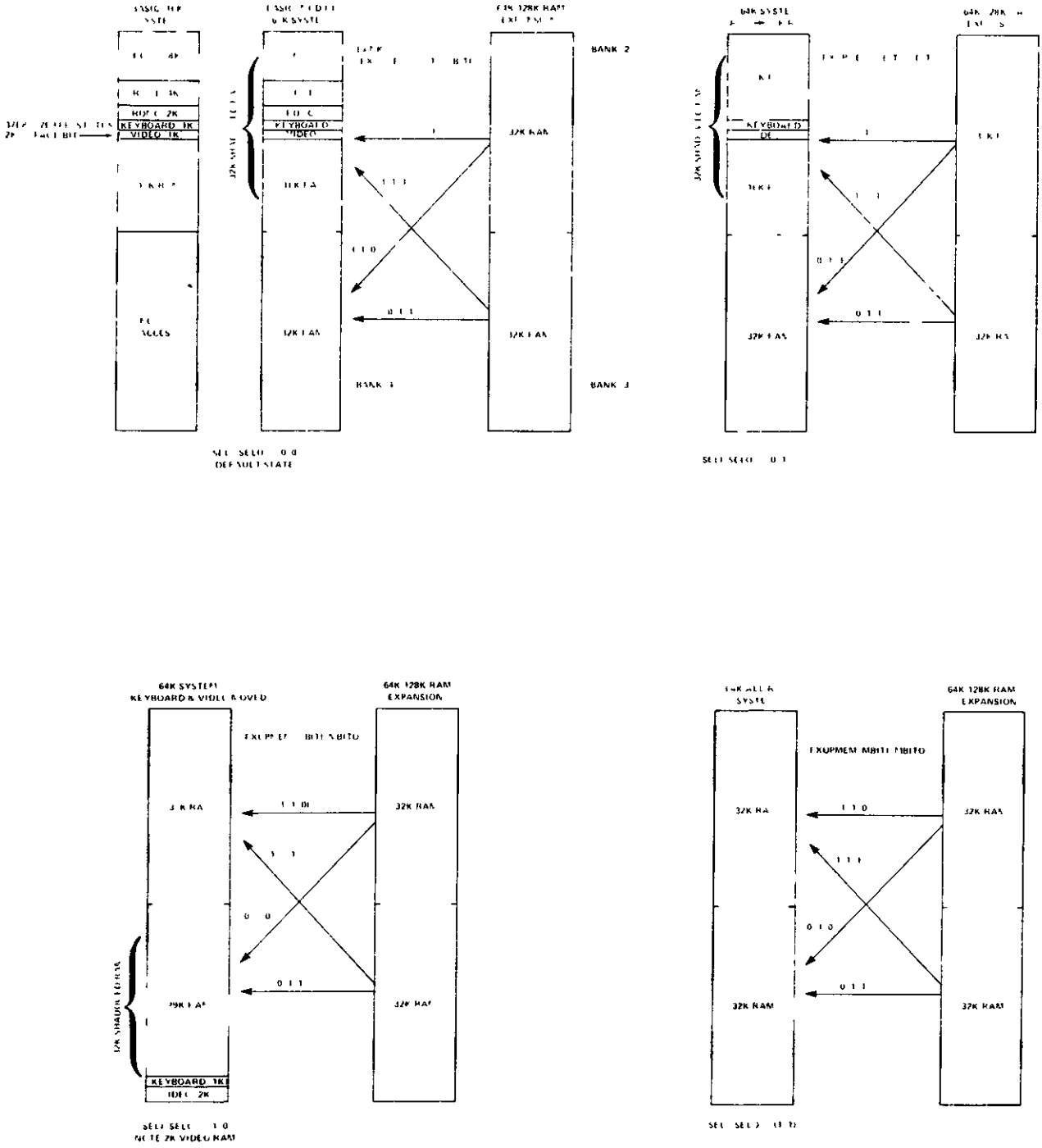


FIGURE 1-2. RAM MEMORY

During screen refresh, the data outputs of the Video RAM (ASCII character codes) are latched by U8 and become the addresses for the character generator ROM (U23) In cases of low resolution graphics a dual 1 of 4 data selector (U9) is the cell generator with additional buffering from U10

The shift register U11 inputs are the latched data outputs of the character or cell generator The shift clock input comes from the PAL U4, and is 10 1376 MHz for the 64 by 16 mode and 12 672 MHz for 80 by 24 operation The serial output from the shift register later becomes actual video dot information

Special timing in the video circuit is handled by hex latch U2 This includes blanking (originating from CRTC) and shift register loading (originating from U4) Additional video control and timing functions, such as sync buffering, inversion selection, dot clock chopping, and graphics disable of normal video are handled by miscellaneous gates in U12, U13, U14, U22, U24, and U26

1.1.9 Real Time Clock

The Real Time Clock circuit in the Model 4 provides a 30 Hz (in the 2 MHz CPU Mode) or 60 Hz (in the 4 MHz CPU Mode) interrupt to the CPU By counting the number of interrupts that have occured, the CPU can keep track of the time The 60 Hz vertical sync signal from the video circuitry is divided by two (2 MHz Mode) by U53, and the 30 Hz at pin 1 of U51 is used to generate the interrupts In the 4 MHz mode, signal FAST places a logic low at pin 1 of U51, causing signal VSYNC to trigger the interrupts at the 60 Hz rate Note that any time interrupts are disabled, the accuracy of the clock suffers

1.1.10 Cassette Circuitry

The cassette write circuitry latches the two LSBs (D0 and D1) for any output to port FF (hex) The outputs of these latches (U27) are then resistor summed to provide three discrete voltage levels (500 Baud only) The firmware toggles the bits to provide an output signal of the desired frequency at the summing node

There are two types of cassette Read circuits – 500 baud and 1500 baud The 500 baud circuit is compatible with both Model 1 and III The input signal is amplified and filtered by Op amps (U43 and U28 Part of U15 then forms a Zero Crossing Detector, the output of which sets the latch U40 A read of Port FF enables buffer U41, which allows the CPU to determine whether the latch has been set, and simultaneously resets the latch The firmware determines by the timing between settings of the latch whether a logic "one" or "zero" was read in from the tape

The 1500 baud cassette read circuit is compatible with the Model III cassette system The incoming signal is compared to a threshold by part of U15 U15's output will then be either high or low and clock about one half of U39, depend ing on whether it is a rising edge or a falling edge If interrupts are enabled, the setting of either latch will gene rate an interrupt As in the 500 baud circuit, the firmware decodes the interrupts into the appropriate data

For any cassette read or write operation, the cassette relay must be closed in order to start the motor of the cassette deck A write to port EC hex with bit one set will set latch U42, which turns on transistor Q4 and energizes the relay K1 A subsequent write to this port with bit one clear will clear the latch and de energize the relay

1.1.11 Printer Circuitry

The printer status lines are read by the CPU by enabling buffer U67 This buffer will be enabled for any input from port F8 or F9, or any memory read from location 37E8 or 37E9 when in the Model III mode For a listing of bit status, refer to the bit map

After the printer driver software determines that the printer is ready to receive another character (by reading the status), the character to be printed is output to port F8 This latches the character into U66, and simultaneouly fires the one shot U65 to provide the appropriate strobe to the printer

1.1.12 I/O Connectors

Two 20 pin single inline connectors, J7 and J8, are provided for the connection of a Floppy Disk Controller and an RS 232 Communications Interface, respectively All eight data lines and the two least significant address lines are routed to these connectors In addition, connections are provided for device or board selection, interrupt enable, interrupt status read, interrupt acknowledge, RESET, and the CPU WAIT signal

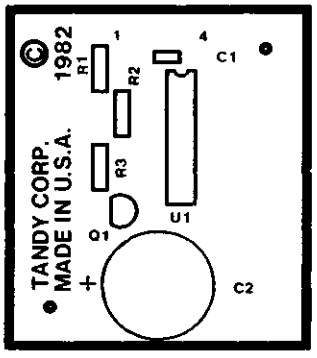
The graphics connector, J10, contains all of the above inter face signals, plus CRTCLK, the dotclock signal, a graphics enable input, and other timing clocks which synchronize the graphics board with the CRTC.

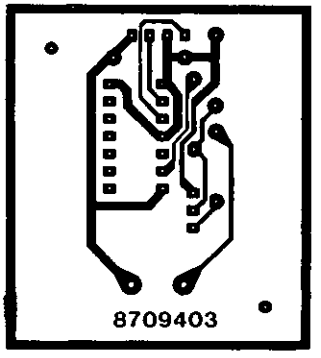
The I/O bus connector, J2, contains connections for all eight data lines (buffered by U74), the low order address lines (buffered by U73), and the control lines (buffered by U75) IN*, OUT*, RESET*, M1*, and IORQ* In addition, the I/O bus connector has inputs to allow the device(s), connected to generate CPU WAIT states and interrupts

The sound connector, J11, contains only four connections: sound enable (any output to port 90 hex), data bit D0, Vcc, and ground.

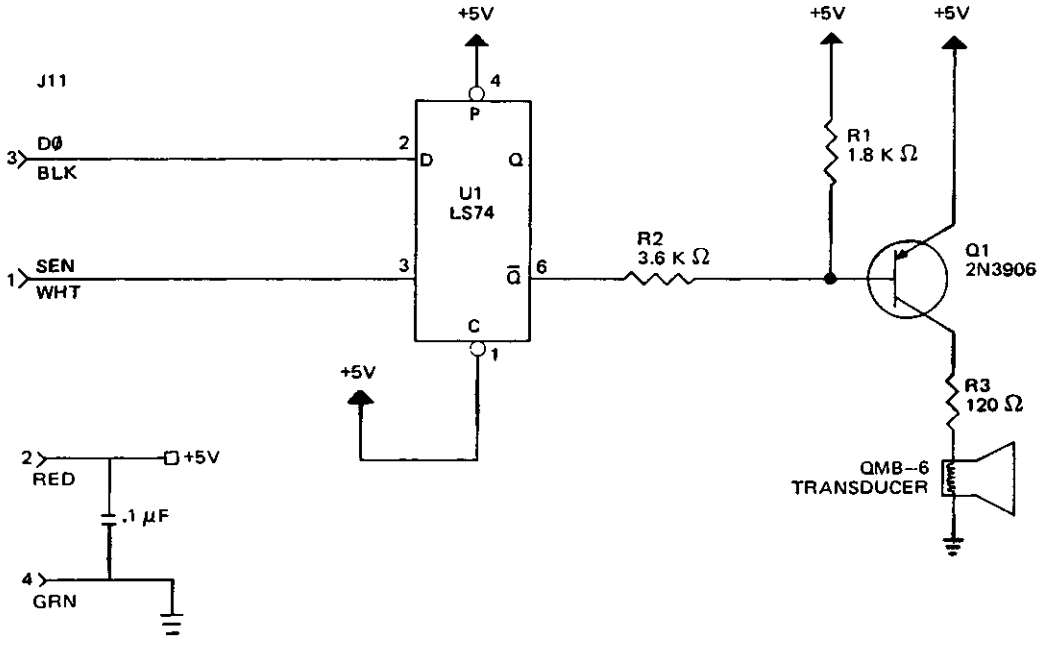
1.1.13 Sound Option

The Model 4 sound option, available as standard equipment on the disk drive versions, is a software intensive device. Data is sent out to port 90H, alternately setting and clearing data bit D0. The state of this bit is latched by sound board U1 and amplified by sound board Q1, which drives a piezoelectric sound transducer. The speed of the software loop determines the frequency, and thus, the pitch of the resulting tone.





COMPONENT LOCATION/CIRCUIT TRACE, SOUND BOARD #8858121



SCHEMATIC 8000188, SOUND BOARD #8858121

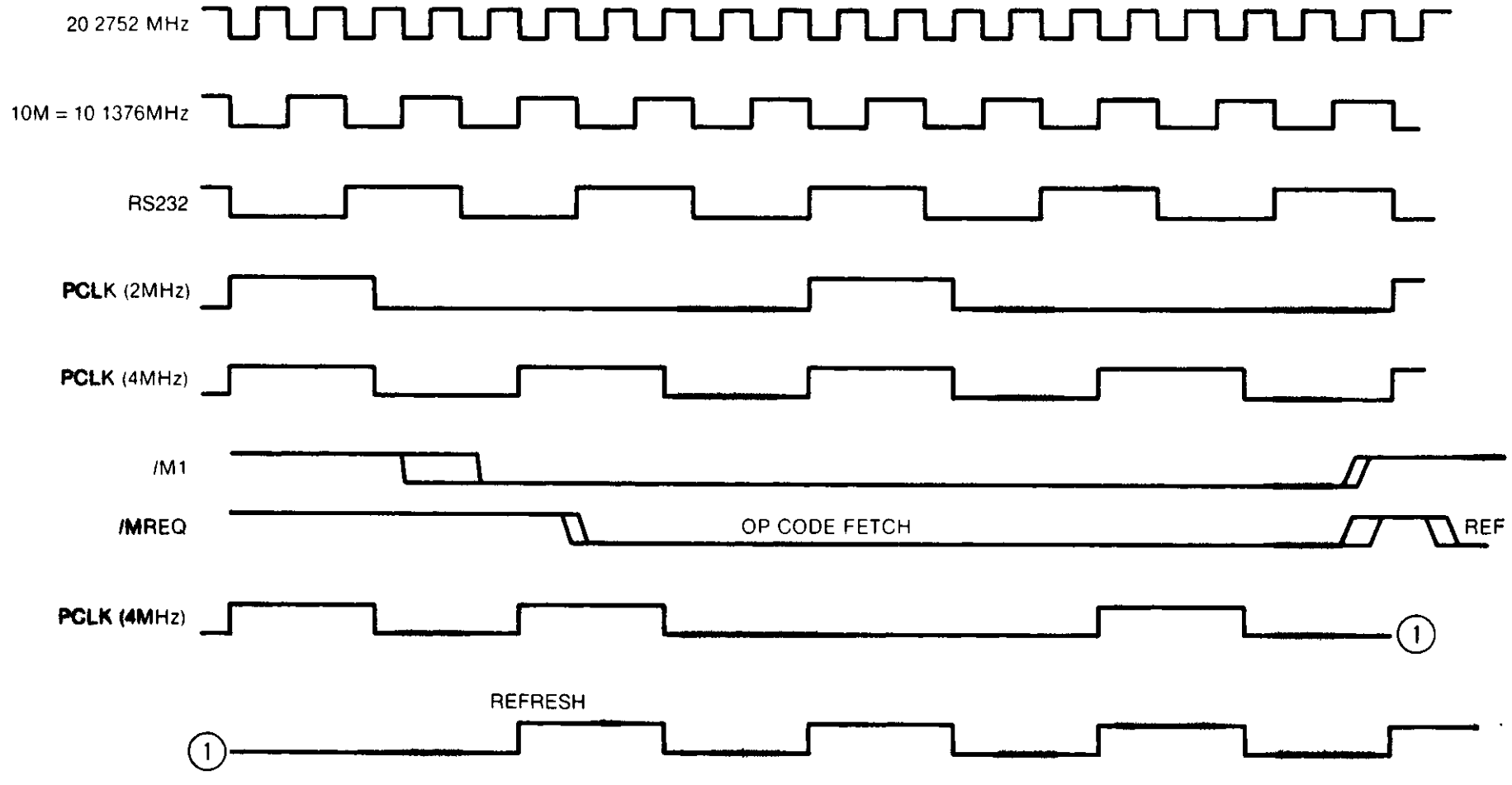


FIGURE 1-3. TIMING OF U3 & CPU

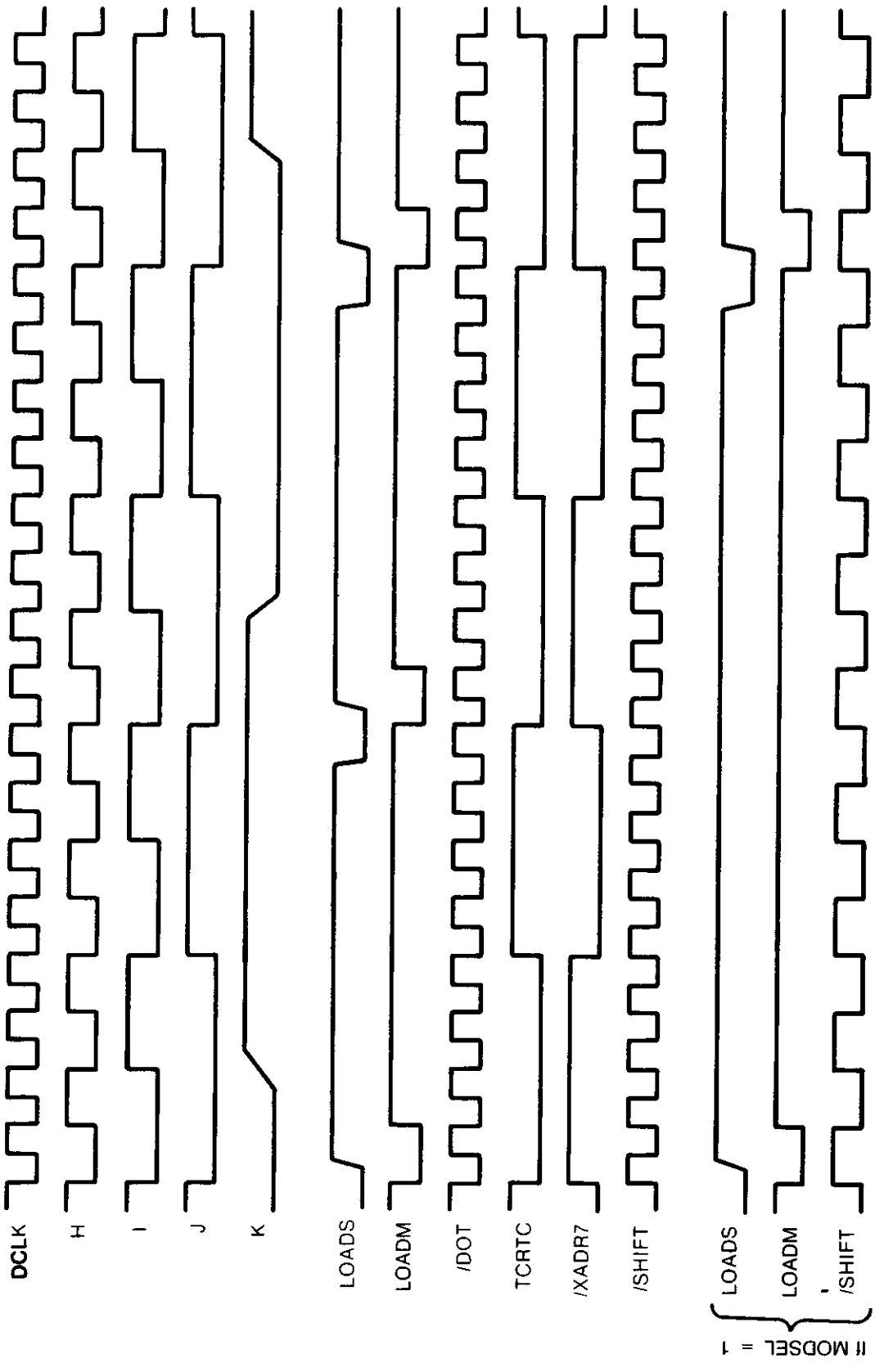


FIGURE 1-4. TIMING OF U4

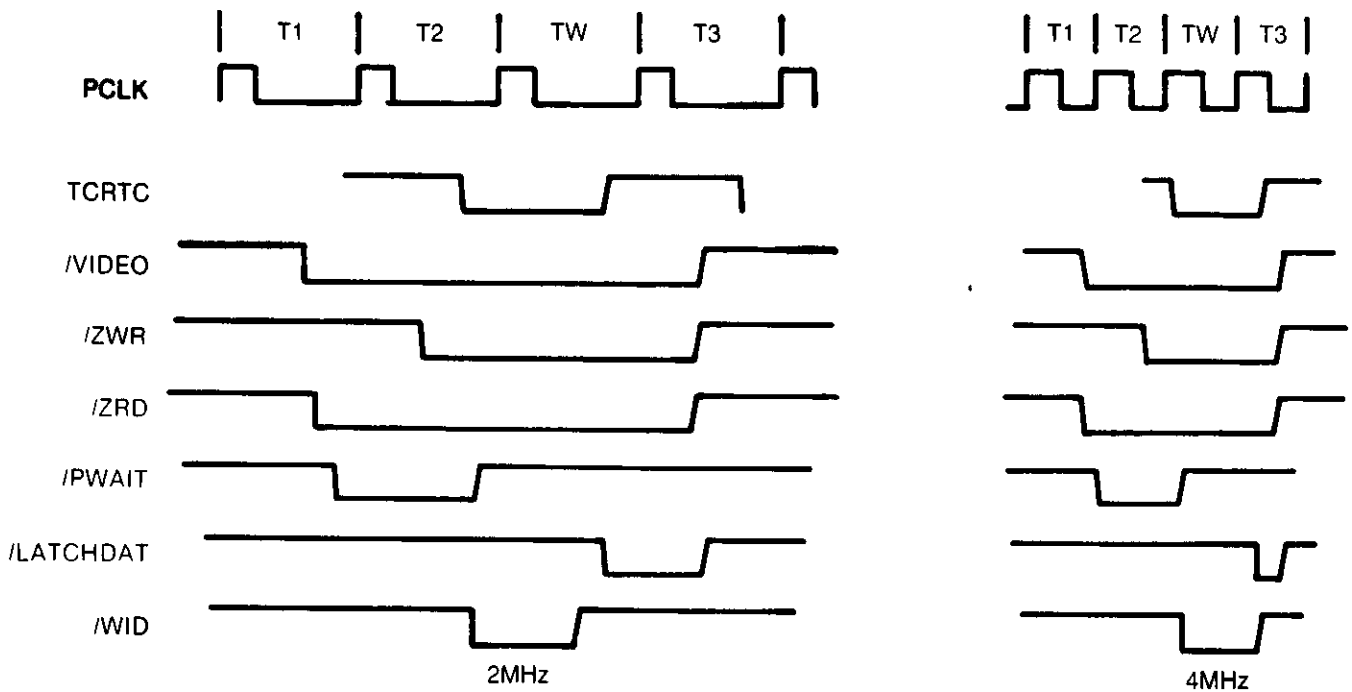


FIGURE 1-6. CPU VIDEO ACCESS TIMING

1.2 MODEL 4 I/O BUS

The Model 4 Bus is designed to allow easy and convenient interfacing of I/O devices to the Model 4 The I/O Bus supports all the signals necessary to implement a device compatible with the Z 80s I/O structure That is

Addresses

A0 to A7 allow selection of up to 256† input and 256 output devices if external I/O is enabled

†Ports 80H to 0FFH are reserved for System use

Data

DB0 to DB7 allow transfer of 8 bit data onto the processor data bus if external I/O is enabled

Control Lines

a IN* – Z 80 signal specifying that an input is in progress Gated with IORQ
b OUT* – Z 80 signal specifying that an output is in progress Gated with IORQ
c RESET* – system reset signal
d IOBUSINT* – input to the CPU signaling an interrupt from an I/O Bus device if I/O Bus interrupts are enabled
e IOBUSWAIT* – input to the CPU wait line allowing I/O Bus device to force wait states on the Z 80 if external I/O is enabled
f EXTIOSEL* – input to CPU which switches the I/O Bus data bus transceiver and allows an INPUT instruction to read I/O Bus data
g M1* – and IORQ* – standard Z 80 signals

The address line, data line, and control lines a to c and e to g are enabled only when the ENEXIO bit in EC is set to a one

To enable I/O interrupts the ENIOBUSINT bit in the CPU IOPORT E0 (output port) must be a one However, even if it is disabled from generating interrupts the status of the IOBUSINT* line can still read on the appropriate bit of CPU IOPORT E0 (input port)

See Model 4 Port Bit assignment for port 0FF 0EC and 0E0 on pages 14 and 15

The Model 4 CPU board is fully protected from "foreign I/O devices" in that all the I/O Bus signals are buffered and can be disabled under software control To attach and use an I/O device on the I/O Bus certain requirements (both hardware and software) must be met

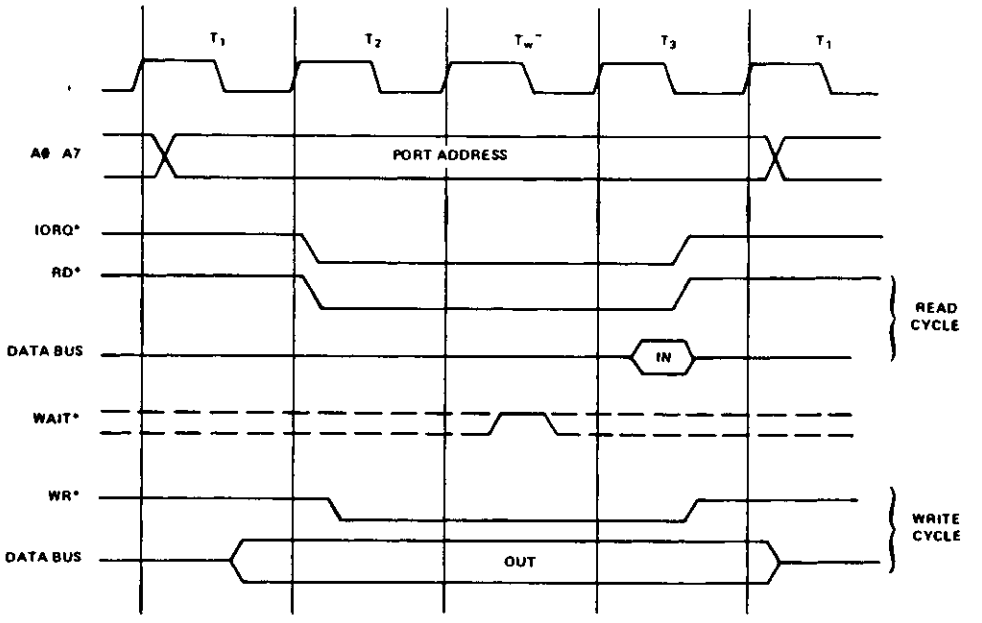
For input port device use you must enable external I/O devices by writing to port 0ECH with bit 4 on in the user software This will enable the data bus address lines and control signals to the I/O Bus edge connector When the input device is selected the hardware will acknowledge by asserting EXTIOSEL* low This switches the data bus transceiver and allows the CPU to read the contents of the I/O Bus data lines See Figure 1 6 for the timing EXTIOSEL* can be generated by NANDing IN and the I/O port address

Output port device use is the same as the input port device in use in that the external I/O devices must be enabled by writing to port 0ECH with bit 4 on in the user software – in the same fashion

For either input or output devices, the IOBUSWAIT* control line can be used in the normal way for synchronizing slow devices to the CPU Note that since dynamic memories are used in the Model 4, the wait line should be used with caution Holding the CPU in a wait state for 2 msec or more may cause loss of memory contents since refresh is inhibited during this time It is recommended that the IOBUSWAIT* line be held active no more than 500 μsec with a 25% duty cycle

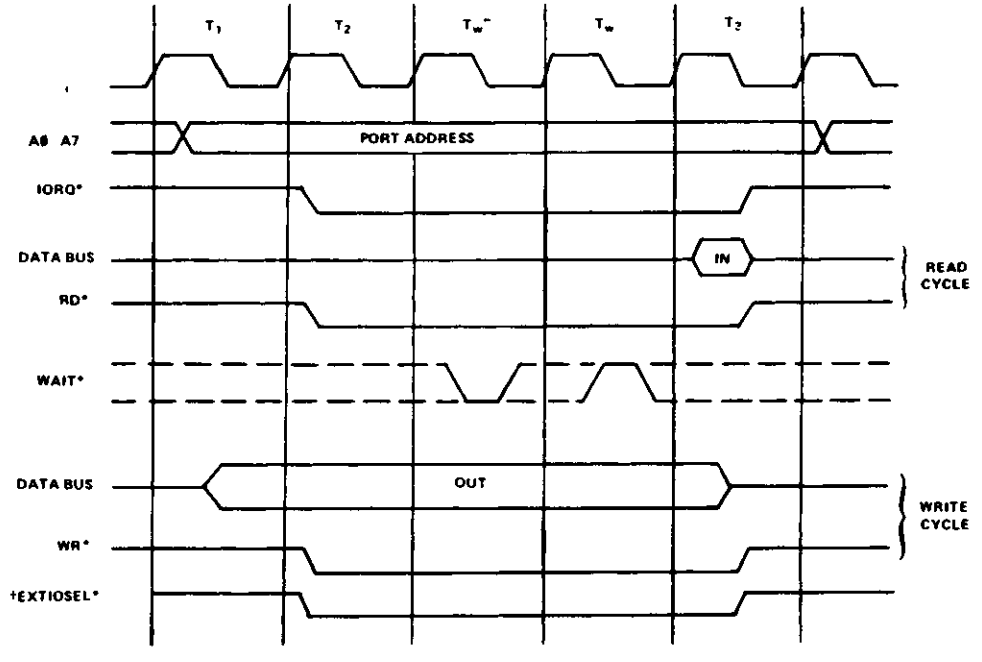
The Model 4 will support Z 80 mode 1 interrupts A RAM jump table is supported by the LEVEL II BASIC ROMs and the user must supply the address of his interrupt service routine by writing this address to locations 403E and 403F When an interrupt occurs the program will be vectored to the user supplied address if I/O Bus interrupts have been enabled To enable I/O Bus interrupts the user must set bit 3 of Port 0E0H

Input or Output Cycles



*Inserted by Z80 CPU

Input or Output Cycles with Wait States.



*Inserted by Z80 CPU

†Coincident with IORQ* only on INPUT cycle

FIGURE 1-6. I/O BUS TIMING DIAGRAM

1.3 MODEL 4 PORT BITS

Name: WRNMIMASKREG*
Port Address: ØE4H
Access: WRITE ONLY

Bit 7 = ENINTRQ; Ø disables Disk INTRQ from generating an NMI.
1 enables above.

Bit 6 = ENDRQ; Ø disables Disk DRQ from generating an NMI.
1 enables above.

Name: RDNMISTATUS*
Port Address: ØE4H
Access: READ ONLY

Bit 7 = Status of Disk INTRQ; 1 = False, Ø = True

Bit 6 = Status of Disk DRQ; 1 = False, Ø = True

Bit 5 = Reset* Status; 1 = False, Ø = True

Name: MOD OUT
Port Address: ØECH
Access: WRITE ONLY

Bit 7 = Undefined

Bit 6 = Undefined

Bit 5 = DISWAIT; Ø disables video waits, 1 enables

Bit 4 = ENEXTIO; Ø disables external IO Bus, 1 enables

Bit 3 = ENALTSET; Ø disables alternate character set,
1 enables alternate video character set.

Bit 2 = MODSEL; Ø enables 64 character mode,
1 enables 32 character mode.

Bit 1 = CASMOTORON; Ø turns cassette motor off,
1 turns cassette motor on.

Bit Ø = Undefined

Name: RDINTSTATUS*
Port Address: ØEØH
Access: READ ONLY

NOTE: A Ø indicates the device is interrupting.

Bit 7 = Undefined

Bit 6 = RS-232 ERROR INT

Bit 5 = RS-232 RCV INT

Bit 4 = RS-232 XMIT INT

Bit 3 = IOBUS INT

Bit 2 = RTC INT

Bit 1 = CASSETTE (1500 Baud) INT F

Bit Ø = CASSETTE (1500 Baud) INT R

Name: CASOUT*
Port Address: ØFFH
Access: WRITE ONLY

Bit 7 = Undefined

Bit 6 = Undefined

Bit 5 = Undefined

Bit 4 = Undefined

Bit 3 = Undfined

Bit 2 = Undefined

Bit 1 = Cassette output level

Bit Ø = Cassette output level

Name WRINTMASKREG*
Port Address 0E0H
Access WRITE ONLY

Bit 7 = Undefined

Bit 6 = ENERRORINT 1 enables RS 232 interrupts on par ity error, framing error, or data overrun error
0 disable above

Bit 5 = ENRCVINT, 1 enables RS 232 receive data register full interrupts,
0 disables above

Bit 4 = ENXMITINT 1 enables RS 232 transmitter holding register empty interrupts,
0 disables above

Bit 3 = ENIOBUSINT, 1 enables I/O Bus interrupts,
0 disables the above

Bit 2 = ENRTC, 1 enables real time clock interrupt,
0 disables above

Bit 1 = ENCASINTF, 1 enables 1500 Baud falling edge inter rupt,
0 disables above

Bit 0 = ENCASINTR 1 enables 1500 Baud rising edge inter rupt,
0 disables above

Name CAS IN*
Port Address 0FFH
Access READ ONLY

Bit 7 = 500 Baud Cassette bit

Bit 6 = Undefined

Bit 5 = DISWAIT (See Port 0ECH definition)

Bit 4 = ENEXTIO (See Port 0ECH definition)

Bit 3 = ENALTSET (See Port 0ECH definition)

Bit 2 - MODSEL (See Port 0ECH definition)

Bit 1 = CASMOTORON (See Port 0ECH definition)

Bit 0 = 1500 Baud Cassette bit

NOTE Reading Port 0FFH clears the 1500 Baud Cassette interrupts

Name DRVSEL*
Port Address 0F4H
Access WRITE ONLY

Bit 7 = FM*/MFM 0 selects single density,
1 selects double density

Bit 6 = WSGEN, 0 - no wait states generated,
1 = wait states generated

Bit 5 = PRECOMP, 0 = no write precompensation,
1 = write precompensation enabled

Bit 4 = SDSEL, 0 selects side 0 of diskette,
1 selects side 1 of diskette

Bit 3 = Drive select 4

Bit 2 = Drive select 3

Bit 1 = Drive select 2

Bit 0 = Drive select 1

SECTION II

4 GATE ARRAY THEORY OF OPERATION

2.1 MODEL 4 GATE ARRAY THEORY OF OPERATION

2.1.1 Introduction

The following discusses each element of the main board of the Model 4 Gate Array block diagram (see Figure 2-1) In each case the intent is understanding the operation on a practical level sufficient to aid in isolating a problem to the failing component

2.1.2 Reset Circuit

Figure 2-2 shows the Reset circuit for generation of reset on power up and when the reset switch is pushed on the keyboard The time constant determined by R8 and C25, is used to allow the system to stabilize before triggering a one shot (U63) with an approximate pulse width of 70 microsecs When the reset switch is pushed, the input pin is brought to ground and fires the one shot when the switch is released

A second point to be noted is the signal POWRS* which is used to reset the drive select latch in the FDC circuit

2.1.3 CPU

The central processing unit of the Model 4 microcomputer is a Z80A microprocessor, and will run in either 2 or 4 MHz mode All of the output lines of the Z80A are buffered The address lines are buffered by two 74LS244s (U2 and U3 with the enable tied to ground), the control lines by a 74F04 (U27), and the data lines by a 74LS245 (U28 with the enable tied to BUSEN* and the direction control tied to BUSDIR*)

2.1.4 System Timing and Control Registers

Control Registers

The first of these registers is the WRINTMASKREG (U34) This is only part of the register as this function is shared with the Gate Array 4 5 The main register contains RTC ENCASINTFALL AND ENCASINTRISE The Gate Array has the interrupts for the RS232C Interface and the I/O bus interrupts and a duplicate of the RTC

The second is the OPREG (U33) which contains the added options of the Model 4 for video and Memory mapping

The last of the registers is MODOUT (U53) and is also readable through the CASSIN (U52) buffer It contains the Cassette motion controls, and the FAST control for Model 4

CPU Clock and RS232 Clock

Most of the timing generation for the board is shown in Figure 2-5 The Gate Array 4 1 1 is the basis for this timing as it produces the 20 2752 MHz clock and then divides this down to produce most of the other clocking functions used on the board

The first clock that is produced is PCLK (pin 23) which drives the CPU It is a divide by ten of the 20 2752 MHz in the 2 MHz mode and a divide by 5 in the 4 MHz mode The transition from one mode to the other is without glitches and both modes are 50 percent duty cycles

Note that the signal that controls this mode also controls the Real Time Clock circuit described later.

As a simple divide by four of the fundamental 20 2752 MHz, the RS232CLK on pin 22 of U9 provides the basic clock to the RS232C circuit

Video and Graphics Clocking and Timing

The timing for both of these functions may be viewed as one since they must operate synchronously and the same timing must be generated for both The additional signals sent to the Graphics Board allow it to maintain synchronization by knowing the phase relation of the signals sent to both of them To further understand the circuit of Figure 2-5 notice the PLL Module (U8) This chip develops a 12 672 MHz signal which is phase locked to the 1 2672 MHz input on pin 5 and is a divide by 16 of the primary 20 2752 MHz clock This provides the Gate Array 4 1 1 with two clocks to drive the video display and the graphics circuits, 10 1376 MHz for 64 character display, and a 12 672 MHz for the 80 character display

The following discussion will consider both the 64 and 80 character displays to be the same, the difference being the primary frequency and not the phase relation or function of the signals generated

The reference clock for the timing is DCLK (U9-15) and the other clocks that are produced for the video output are derived from this clock (DOT* at U9-17 is a phase shift of DCLK and is provided as an option for the the dot clock for variations in delay paths in the video section) U9 then generates SHIFT* (pin 21), XADR7* (pin 20), CRTCLK (pin 19), LOADS* (pin 18), and LOAD* (pin 16) for the proper timing for the four video modes In addition for the Graphics Board to synchronize with this timing H (pin 14), I (pin 13), and J (pin 11) are fed to connector J12 See Figures 2-6 and 2-7 for the timing diagrams for video clocks generated by Gate Array 4 1 1

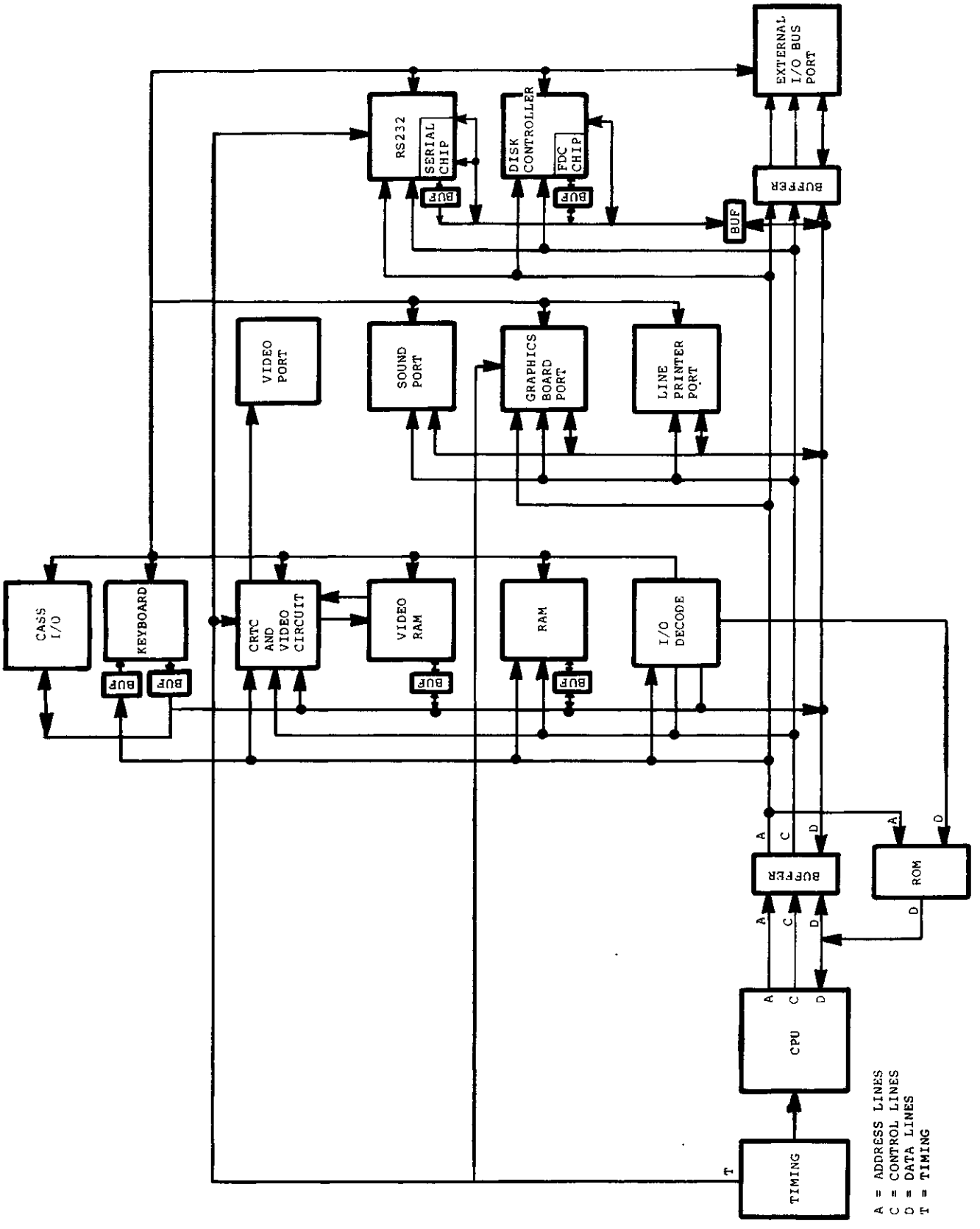


Figure 2-1. Model 4 Gate Array Functional Block

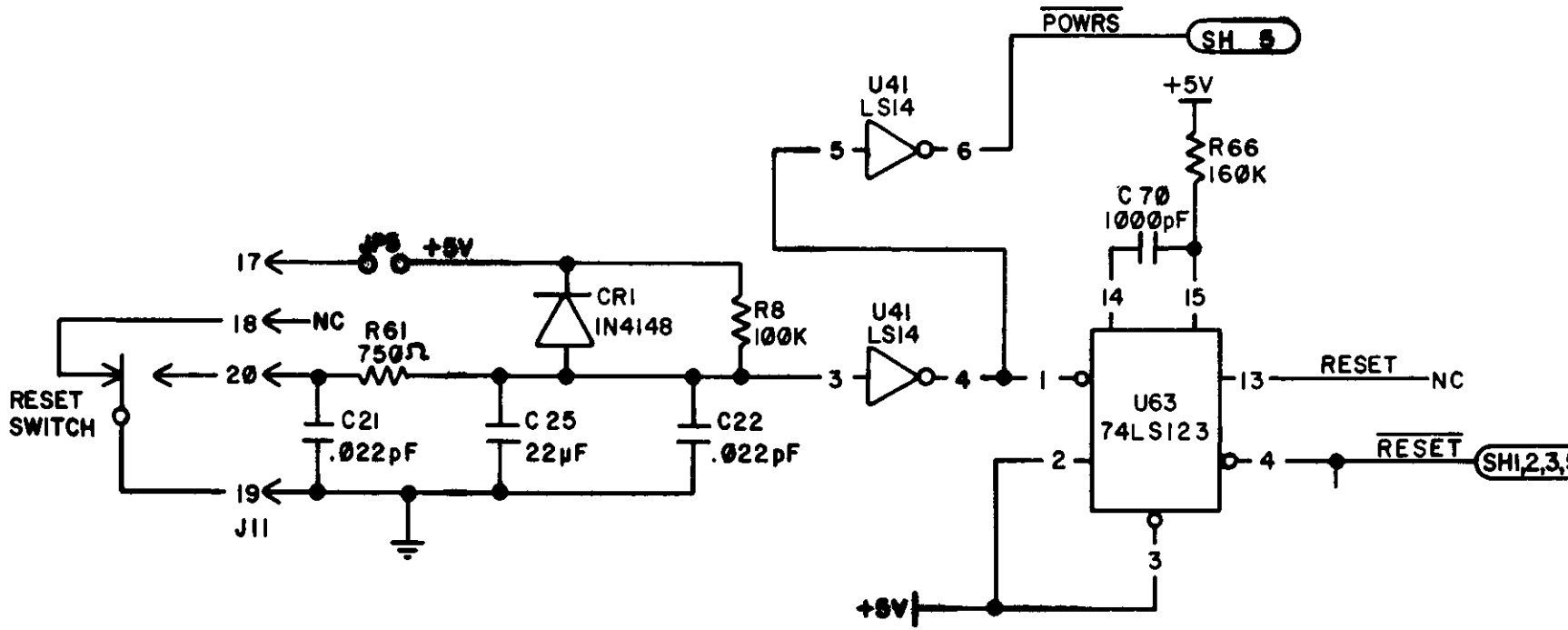


Figure 2-2. Reset Circuit

(Page 4 of Schematic)

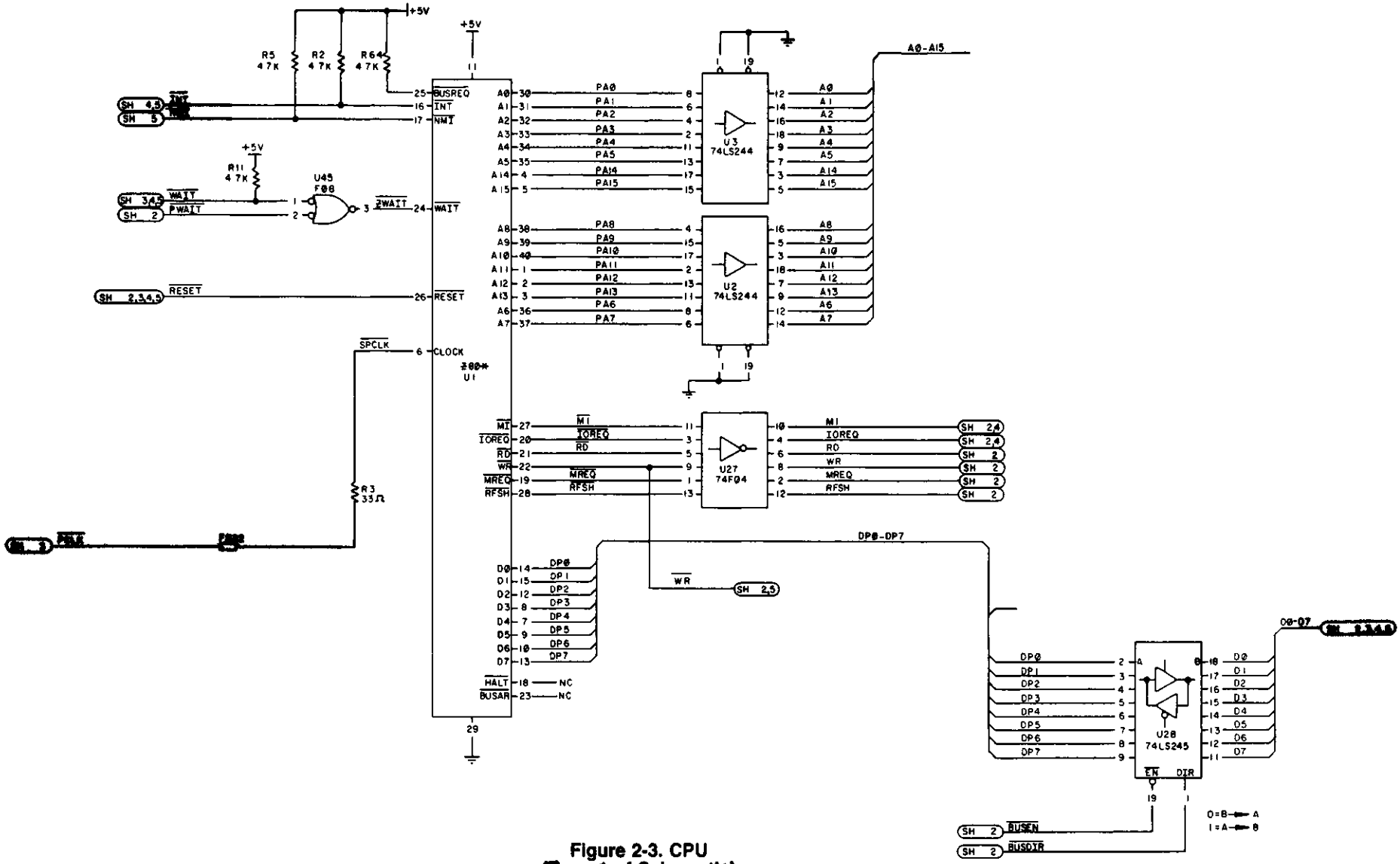


Figure 2-3. CPU
(Page 1 of Schematic)

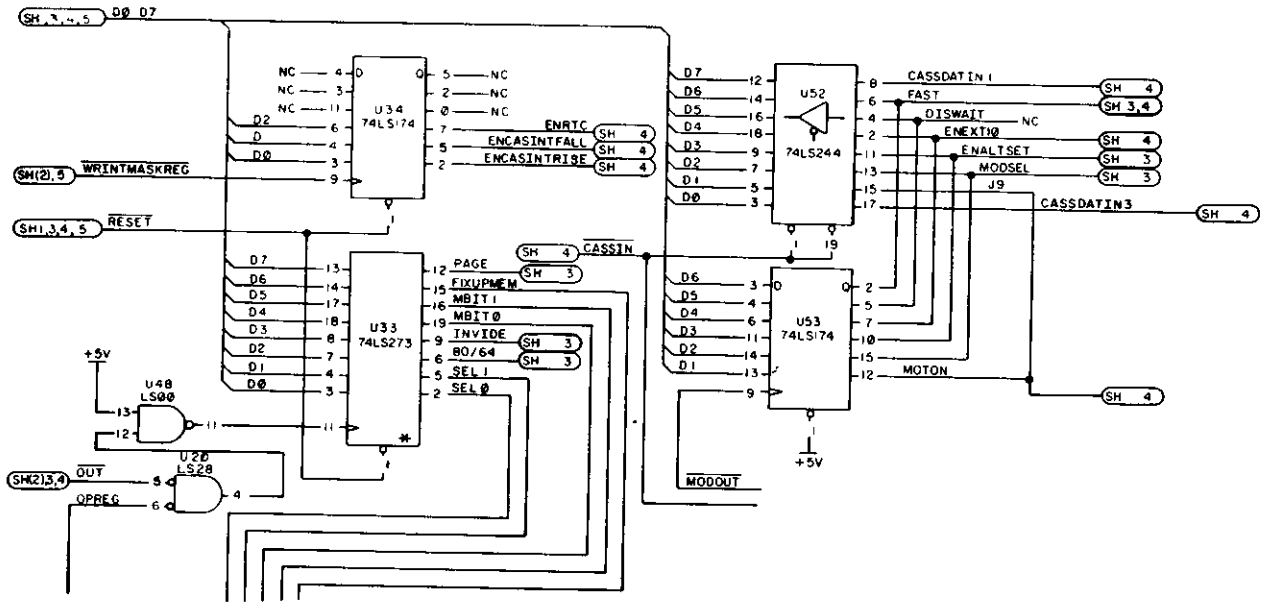


Figure 2-4. Control Registers
(Page 2 of Schematic)

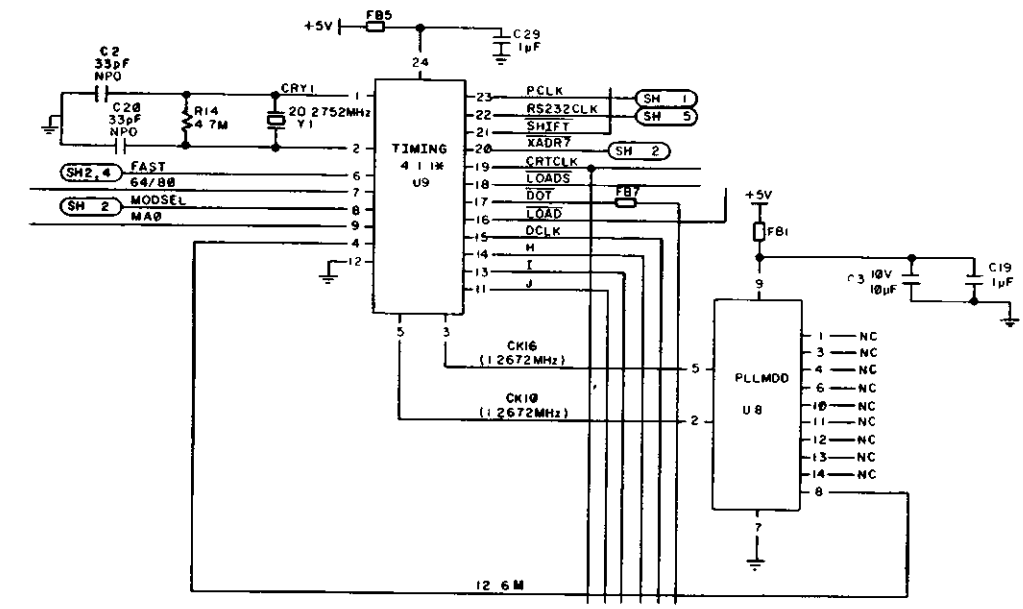


Figure 2-5. CPU, RS232C, and Video Timing Generation
(Page 3 of Schematic)

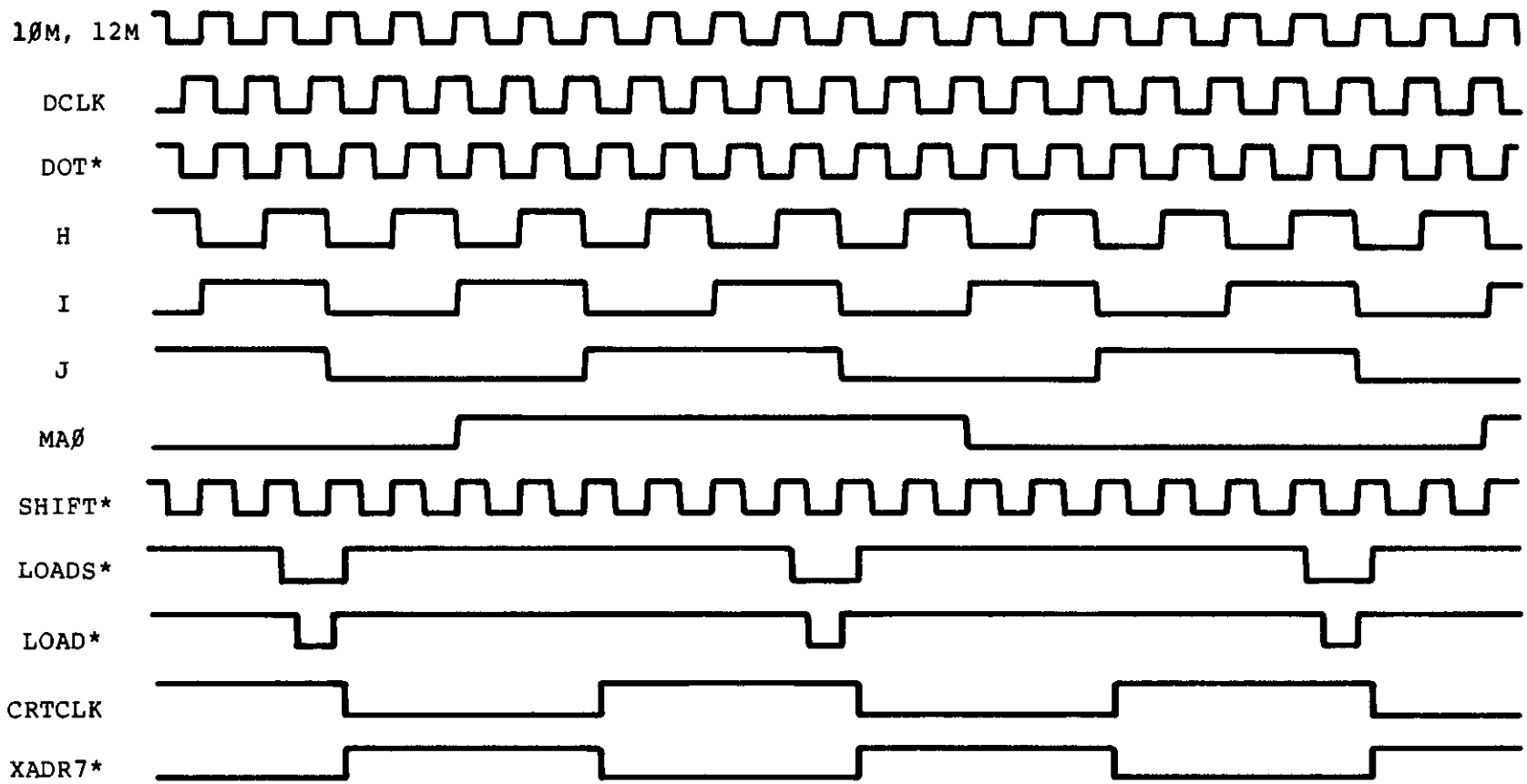


Figure 2-8. Video Timing 64 x 16 Mode 80 x 24 Mode

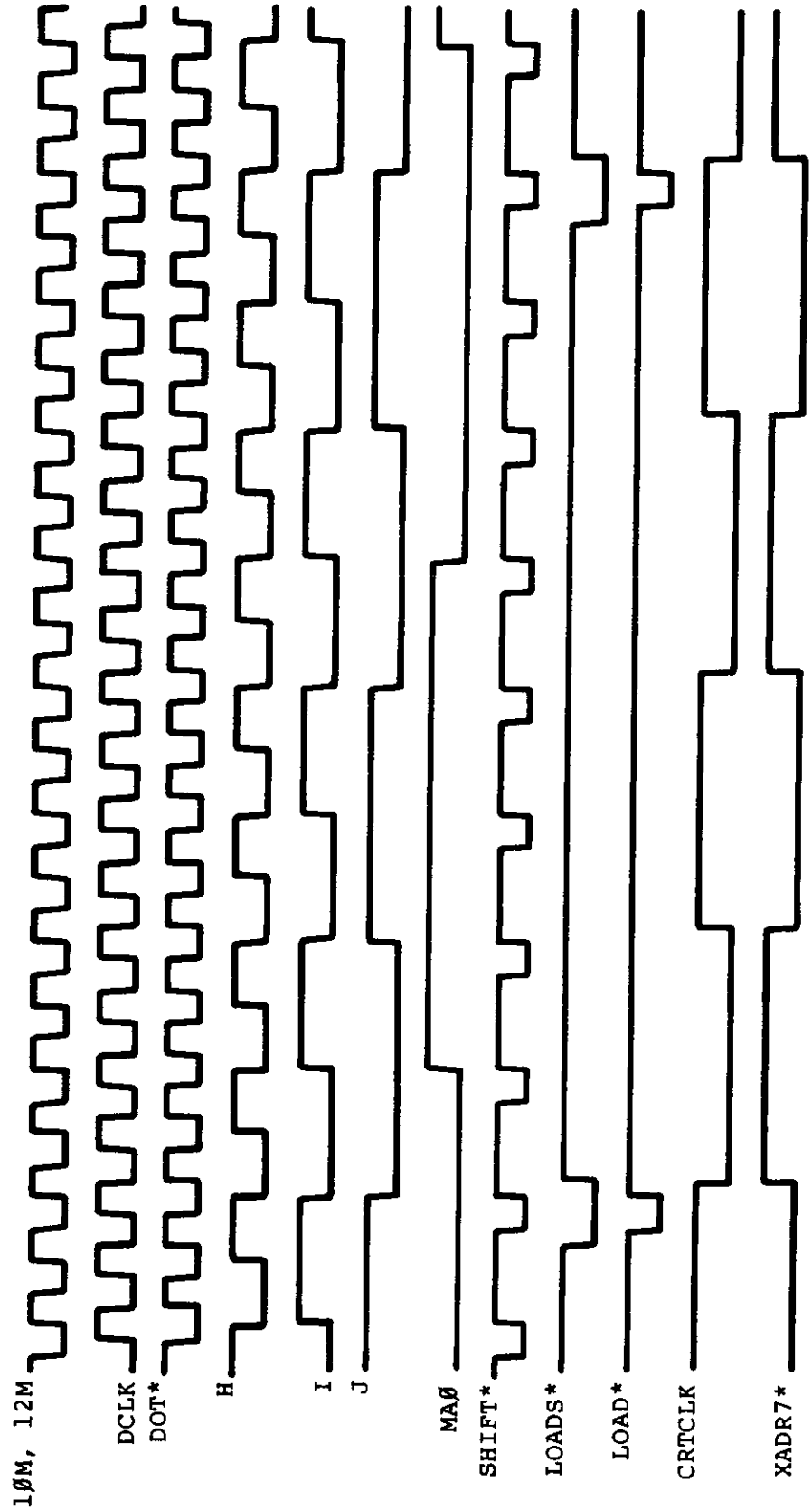


Figure 2-7.

DRAM and Video RAM Timing

The Video RAM and DRAM timing share the timing delay line (U80) This is done by 'OR''ing the two signals GRAS* and AINPRG* at U39 to get the signal STDEL* This is possible because the signals VIDEO and MREQ or MCYCEN are gated in to mask off the signals that are not desired.

Since the CRTC and the CPU are operating independently and at different clock rates, when the CPU wants to access the Video RAM the two must synchronize with each other This is accomplished when a video access is decoded WAIT* it is pulled low, when it is determined whether the access is a read or write and the correct cycle of the CRTC clock is present, the actual access can begin, hence AINPRG* is generated and WAIT* is released

From this point the actual sequence depends on whether a read or a write is done On a read the address is enabled to the RAM, the delay through U80 to VLATCH* when data is latched in the 74LS373 where the CPU can pick-up the data at the completion of this cycle On a write the sequence is more complex The address is enabled to the RAM, the output is disabled (VRAMDIS* at U7-12), write is delayed with respect to the address (DLYWR* at U60-6) and the buffer on the data lines is enabled (VBUFEN* at U60-8), then after a delay the write is cutoff to end the cycle for the RAM (ENDVW* at U80-10) For the timing diagram of the Video RAM CPU access see Figure 2-8

DRAM Timing

The DRAM timing is shown in Figure 2-9 At the begining of the CPU cycle the address lines settle-out first and are, therefore, decoded to allow maximum access speed (see Address Decode) With the generation of MREQ, U39-11 generates PMREQ and enables U42 and gates this with the type of cycle to develop GRAS* (U30-6), RAS0* (U30-3), and RAS1* (U30-11) GRAS* is then "OR"ed with AINPRG as mentioned above The timing from this point is very straight forward With RAS0* and RAS1* generated next MUX (U80-12) is built to switch the addresses to memory then GCAS is generated and clocks flip-flop U31 with MCYEN on the J term This is done to make sure this is a true memory cycle Then if this is an M1 cycle VLATCH* clocks at U31 and cuts off PMREQ* at U39 to end the cycle For timing diagrams of the memory interface see Figures 2-10 to 2-12

2.1.5. Address Decode

This section is divided into two parts, the memory addressing and the I/O addressing This separation is a reflection of the separate mapping of memory and I/O of the Z80A itself For reference of both sections, see Figure 2-13

Memory Address

The memory map for the Model 4 is shown in Table 2-1 and is best described as an option overlay in the sense that at each step of additional memory, the new options overlap the previous and the new options are added on Moreover, the added options have no effect on previous levels and are invisible at those levels.

Address in hex				
MAP I*	**MAP II**	**MAP III**	**MAP IV**	**Function of block**
	0000-37FF	0000-F3FF	0000-FFFF	RAM (64K)
0000-37E7				ROM
37E8-37E9				Printer Status
37EA-37FF				ROM
3800-3BFF	3800-3BFF	F400-F7FF		Keyboard
3C00-3FFF**	3C00-3FFF**	F800-FFFF		Video RAM
4000-7FFF				RAM (16K)
4000-FFFF	4000-FFFF			RAM (64K)

Table 2-1

* Only map available on 16K machine
** Page bit is used to select 1K of 2K Video RAM

The decoding of the addresses for the memory map described above is done for the most part by U5 The only decode not done by U5 is the line printer memory status port at 37E8 and 37E9 hex These needed additional address lines hence the decode LPADD as an input to U5

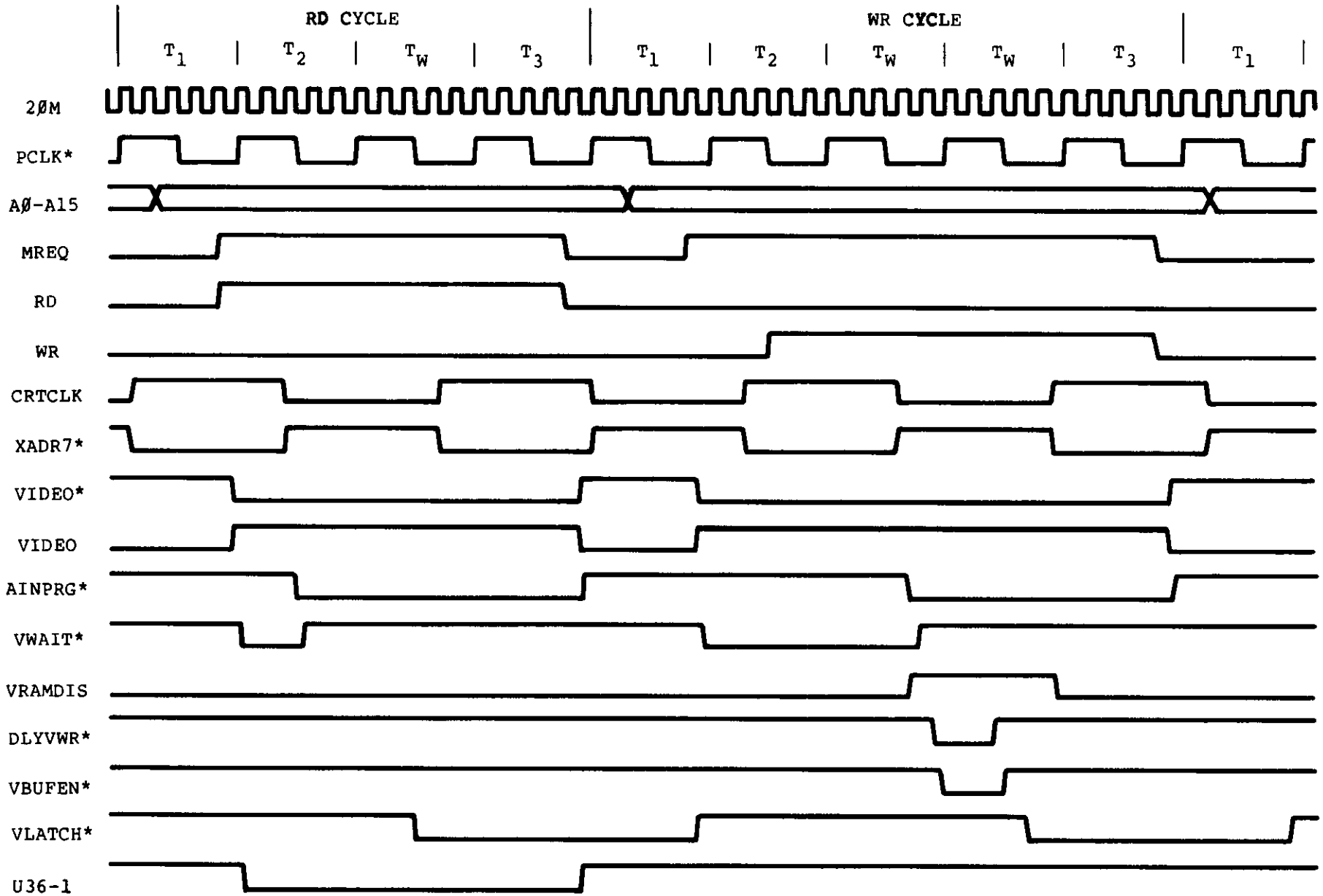


Figure 2-8. Video RAM CPU Access Timing

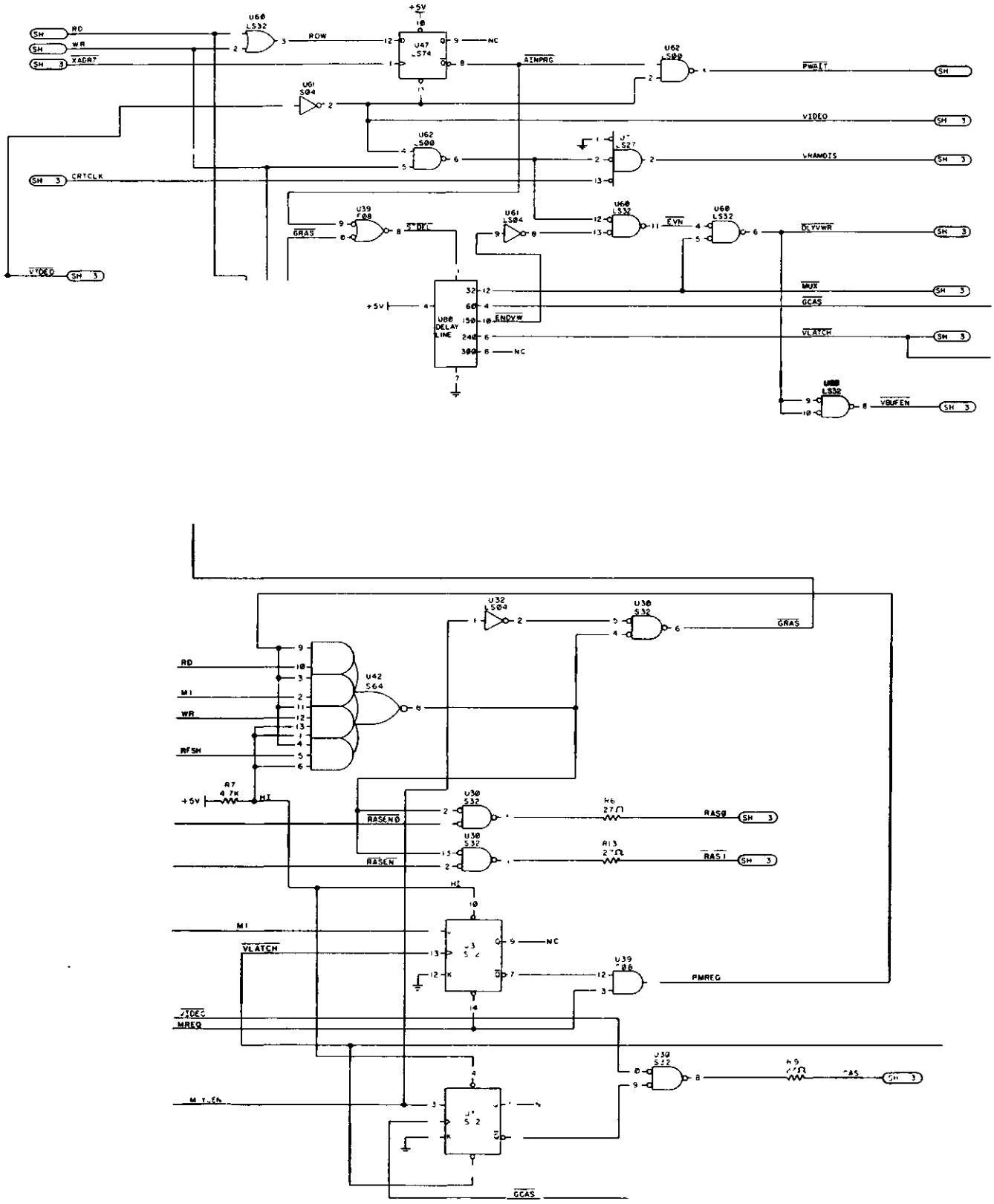
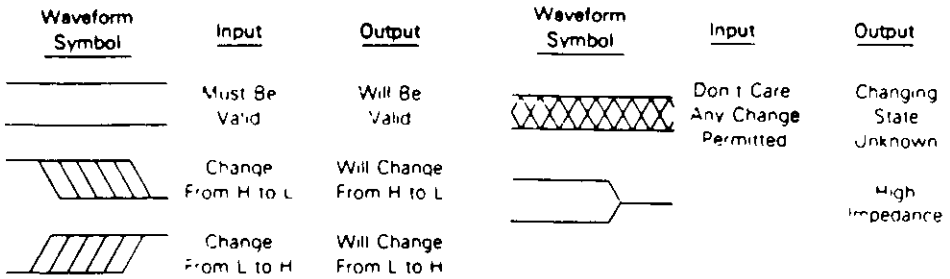


Figure 2-9. Video RAM and DRAM Timing Circuit.

(Page 2 of Schematic)



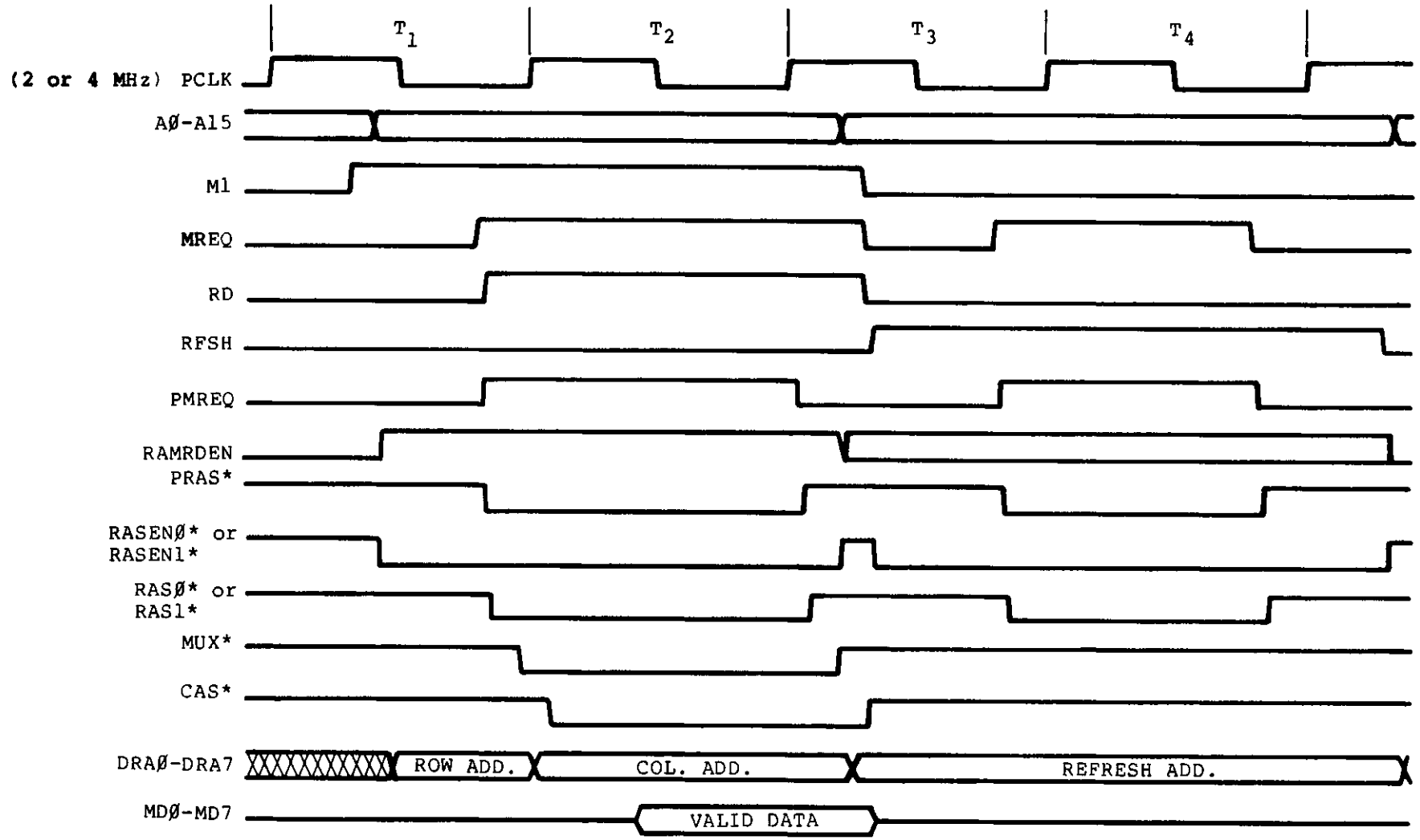


Figure 2-10. M1 Cycle Timing

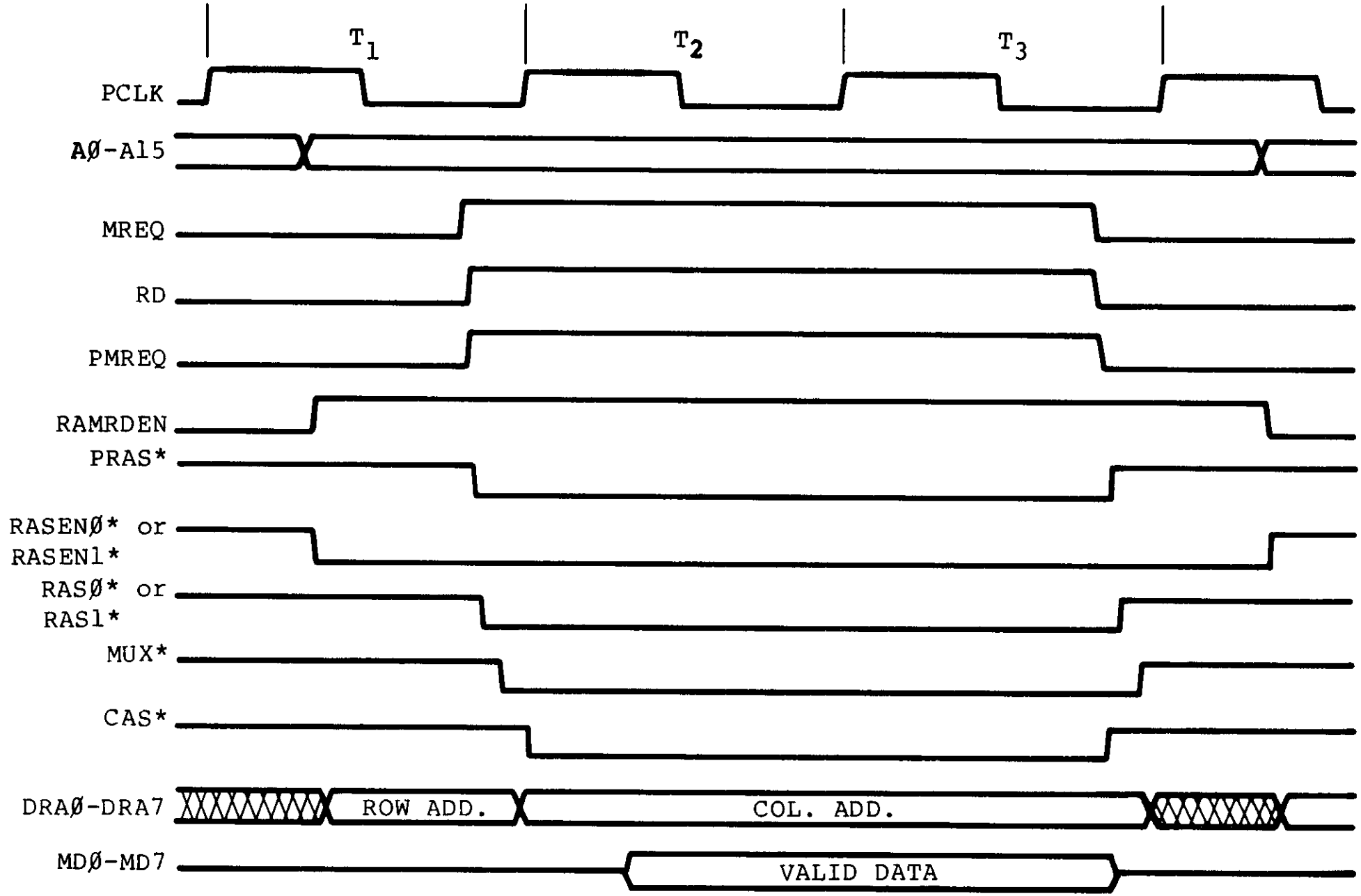


Figure 2-11. Memory Read Cycle Timing

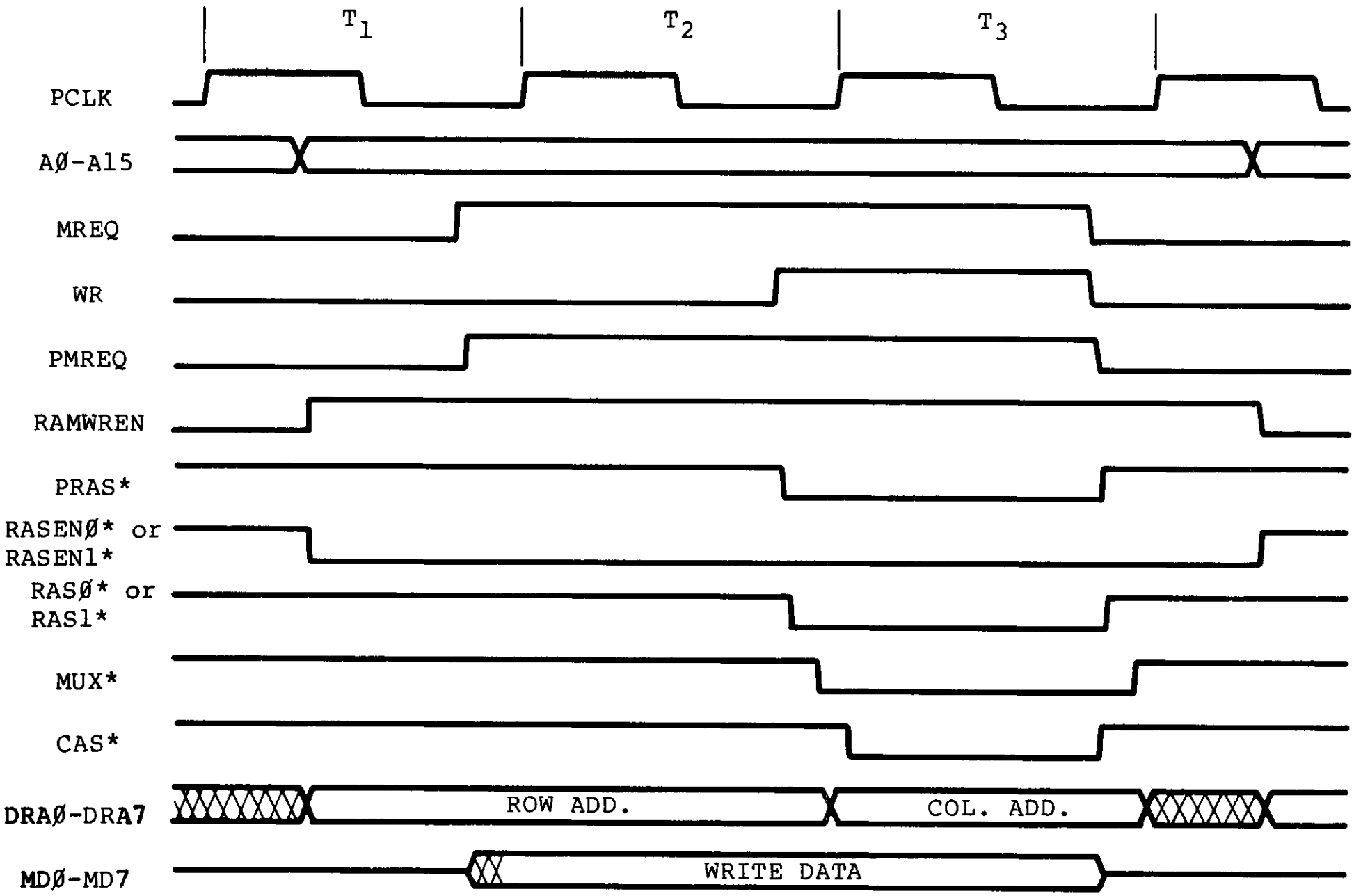


Figure 2-12. Memory Write Cycle Timing

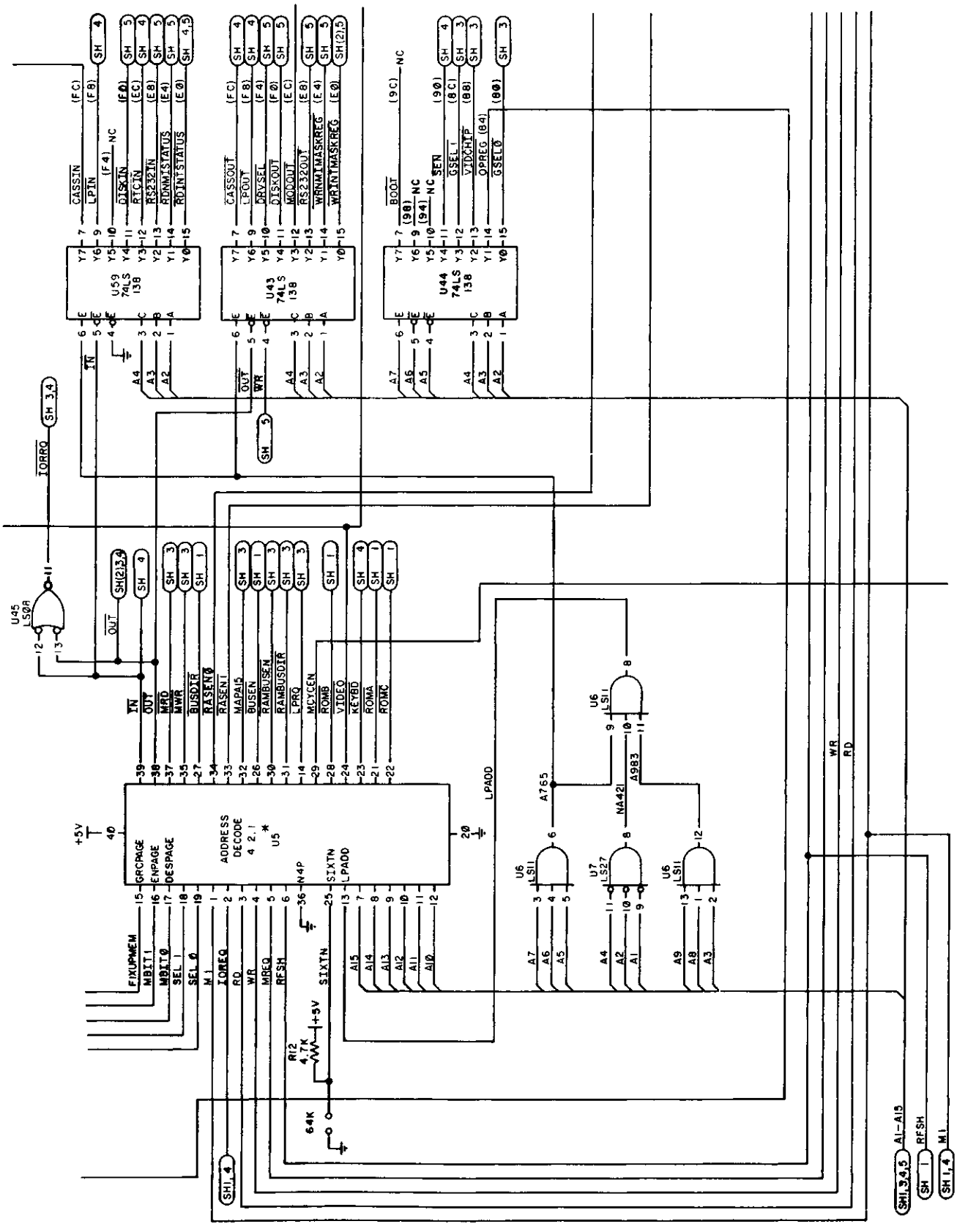
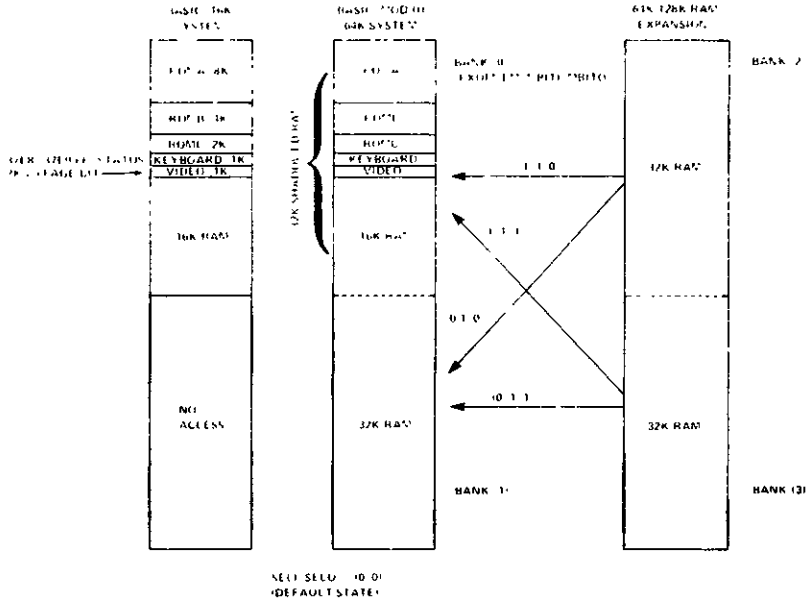
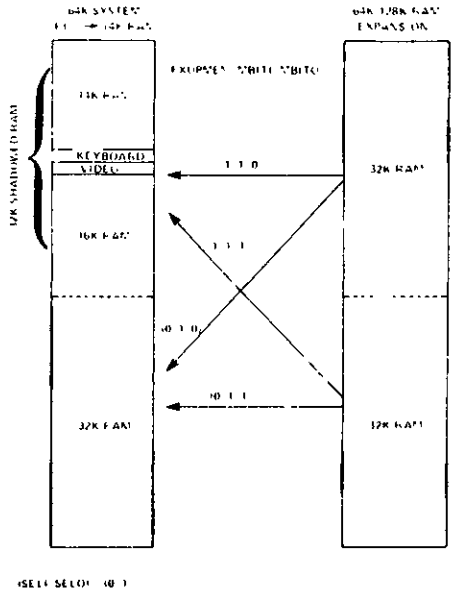
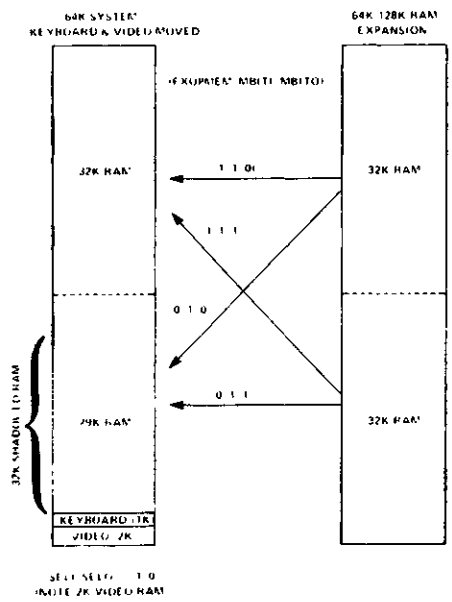


Figure 2-13. Address Decode (Page 2 of Schematic)







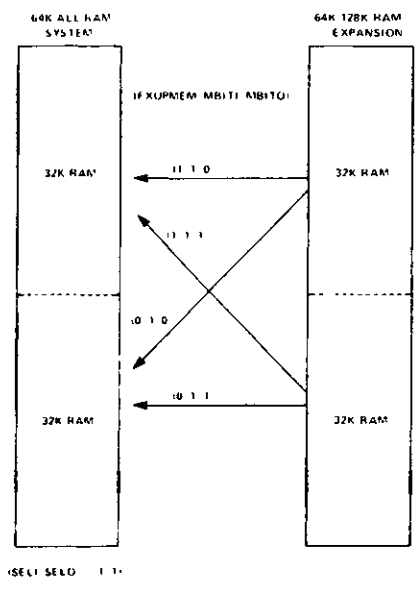


Table 2-2. RAM Memory

I/O port Address

The Port Map decoding is accomplished by three 74LS138s (U43,U44, and U59) These ICs decode the low order address lines (A0 – A7) from the CPU and decode the port being selected The IN* signal and OUT* signal are used in the decode for U59 and U43, but U44 is a pure address decode and, therefore, needs to be gated with IN*, OUT*, or IOREQ* later For a complete I/O map see Table 2-3

2.1.6. ROM

The A ROM is enabled by the decode as appropriate by the address logic described above, and is addressed in a simple straight forward fashion The enable for the B/C ROM is also similarly accomplished, however, the address has a jumper option available This option is designed to allow for testing of the board logic in the factory When jumper is moved from JP8 to JP7, the ROM is in the test mode, with the options appearing on the screen

2.1.7 DRAM

The DRAM timing was described earlier in the timing section, the actual DRAM is contained in two banks of eight each U65 to U74 and U85 to U92 They are arranged in order of data bits D0 through D7, U65 and U85 being D0, through U74 and U92 being D7 Note in Figure 2-15 that the two banks are different with jumper options in the lower bank, these options are for the possible use of 16k three voltage parts When jumpered as shown in Figure 2-14 the bank is identical to the second bank and is for using 64k DRAMs With both banks filled there is 128k available to the user

2.1.8 Video Circuit

Video Modes

The Model 4 has many video options available through hardware and software Software has control of inverse video on a character by character basis by turning on INVIDE Note that this implies the available number of characters is now 128 since the most significant bit of the character code in memory is now used to indicate inverse character Similarly, an alternate character set can be enabled by turning on ENALTSET This enables a new 64 characters in place of the last 64 characters, that is, the Kana set in place of the game set An option not available to software is an enhanced character, which moves characters down one row in their character block to make an inverse character appear within the inverse block and not on the edge of the block This is done by moving jumper JP11 to JP12 As an example of a combination of hardware and software options available in the video is the overlay, which not only requires the Graphics Board to be installed, but also software to enable the graphics data and the video data with text at the same time

The Model 4 also has an option for either 64 character or 80 character wide screen The 64 character screen is compatible with the Model III and displays 16 lines The 80 character screen displays 24 lines In addition each of these has a double width mode These options are controlled by two bits, MODSEL and 8064 which provide the screens as shown in the following table

8064	MODSEL	Video Screen Size
0	0	64 x 16
0	1	32 x 16
1	0	80 x 24
1	1	40 x 24

Table 2-4

With this information of the options available to the user we can now view the actual operation of the circuit with the final objectives in mind and see how they are achieved For the rest of this section all references will be made to Figure 2-16 The first task to be accomplished would be the screen refresh and this is done by the CRTC or 68045 (U11) which will generate the addresses continuously on its address lines Then to allow the CPU access to the same memory the address lines are multiplexed at U12, U14, and U15 on opposite phases of the CRT clock The CPUs access timing is then handed by the timing circuit described earlier

The data bus of the RAM (U16) is a two way bus with the RAM as a source or destination on all accesses, the video gate array (U17) is the destination on the screen refresh half of the cycle, the 74LS373 (U36) is the destination on a read of the RAM by the CPU, and the 74LS244 (U35) is the source on writes to the RAM

The video gate array then gates the RAM data INVIDE, and ENALTSET to determine the ROM addressing for these two options and CHRADD to the 74LS283 (U13) which takes the row address from the 68045 and adds a zero to the row address or a minus one to form the character enhanced mode

The data out of the ROM is then sent back to the gate array where it is then changed to a serial stream of data which is synchronized with the data that would come from the graphics board, GRAFVID The signal CL166 will inhibit the data out of the serial register and the signal ENGRAF enables the graphics data, hence, if both are enabled the effect is an overlay The output data is sent to U20 pin 9 where it is gated with one of two phases of the dot clock, then after being filtered to lower the R F I it is output to the sweep board

Model 4 Port Bit Map

Port	D7	D6	D5	D4	D3	D2	D1	D0
FC - FF	Cass							Cassette
(READ)	data 500 bd			(MIRROR of PORT EC)				data 1500 bd
FC - FF			(Note, also resets cassette data latch)				cass.	cassette
(WRITE)	x	x	x	x	x	x	out	data out
F8 - FB (READ)	Prntr BUSY	Prntr Paper	Prntr Select	Prntr Fault	x	x	x	x
F8 - FB (WRITE)	Prntr D7	Prntr D6	Prntr D5	Prntr D4	Prntr D3	Prntr D2	Prntr D1	Prntr D0
EC - EF			(Any Read causes reset of Real Time Clock Interrupt)					
EC - EF (WRITE)	x x	CPU Fast	x x	Enable EX I/O	Enable Altset	Mode Select	Cass Mot On	x x
E0 - E3 (READ)	x x	Receive Error	Receive Data	Xmit Empty	10 Bus Int	RTC Int	C Fall Int	C Rise Int
E0 - E3 (WRITE)	x x	Enable Rec Err	Enable Rec Data	Enable Xmit Emp	Enable 10 Int	Enable RT Int	Enable CF Int	Enable CR Int
90 - 93 (WRITE)	x x	x x	x x	x x	x x	x x	x x	Sound Bit
84 - 87 (WRITE)	Page	Fix Upr Memory	Memory Bit 1	Memory Bit 0	Invert Video	80/64	Select Bit 1	Select Bit 0

Table 2-3. I/O Port Map

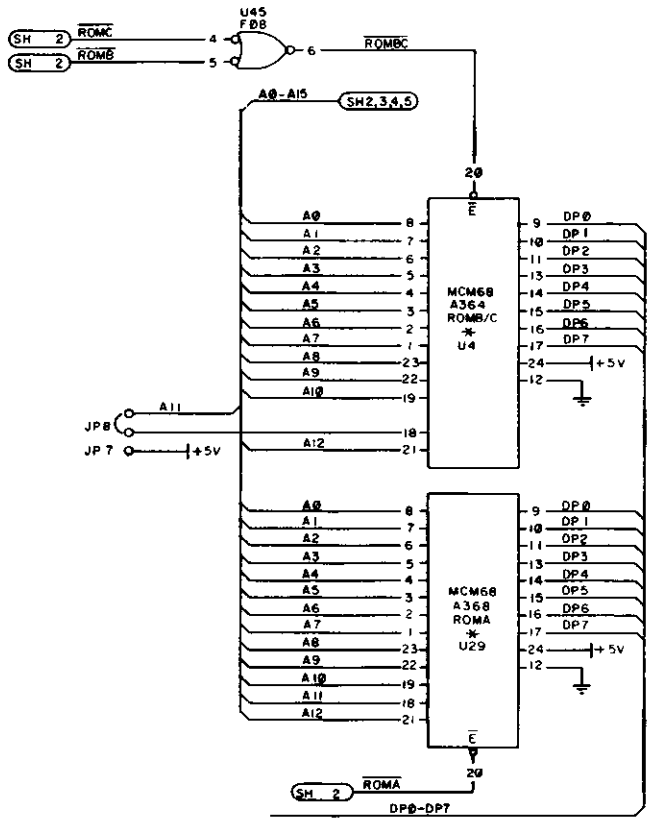


Figure 2-14. ROM Circuit

(Page 1 of Schematic)

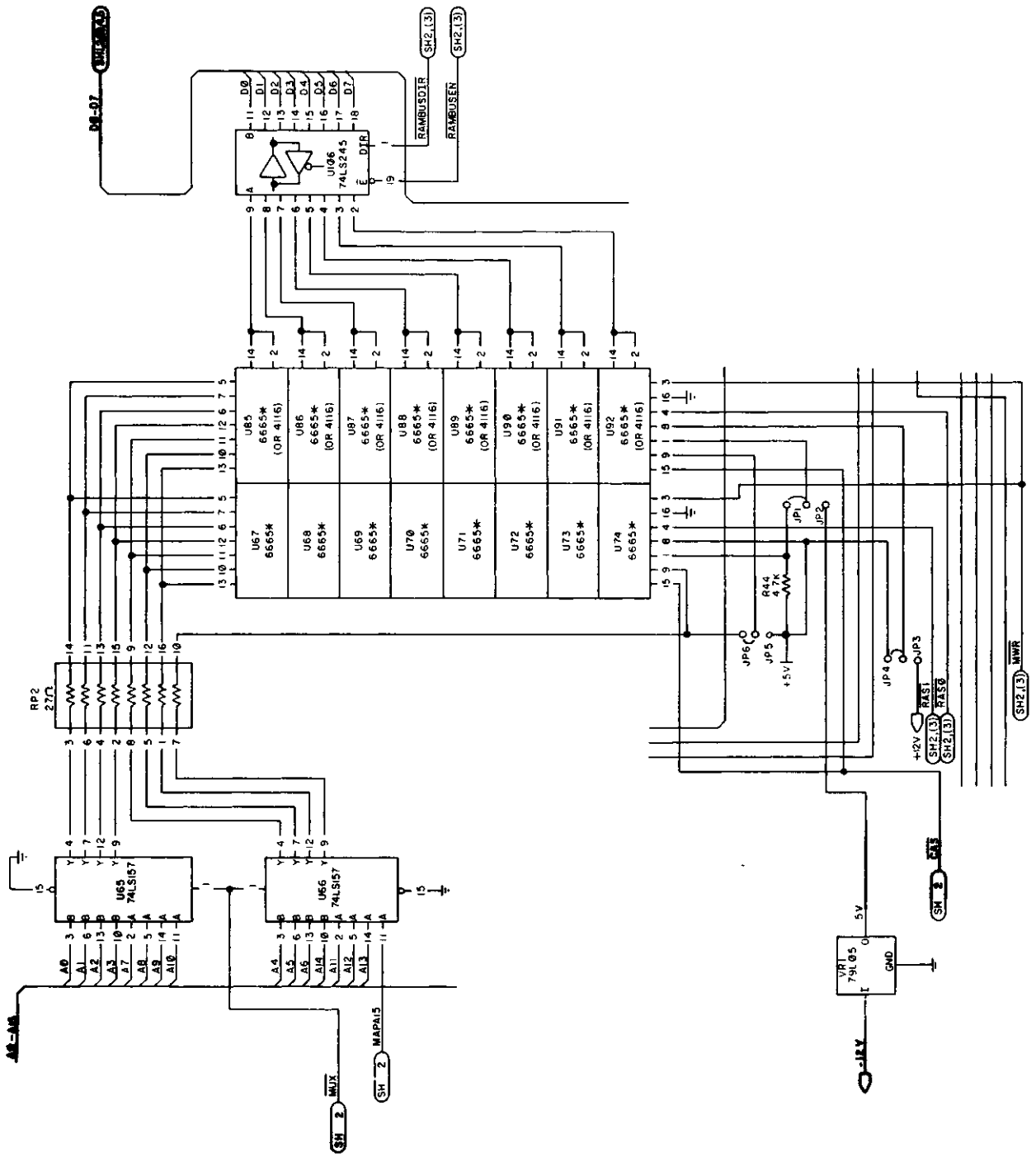


Figure 2-15. DRAM Circuit

(Page 3 of Schematic)

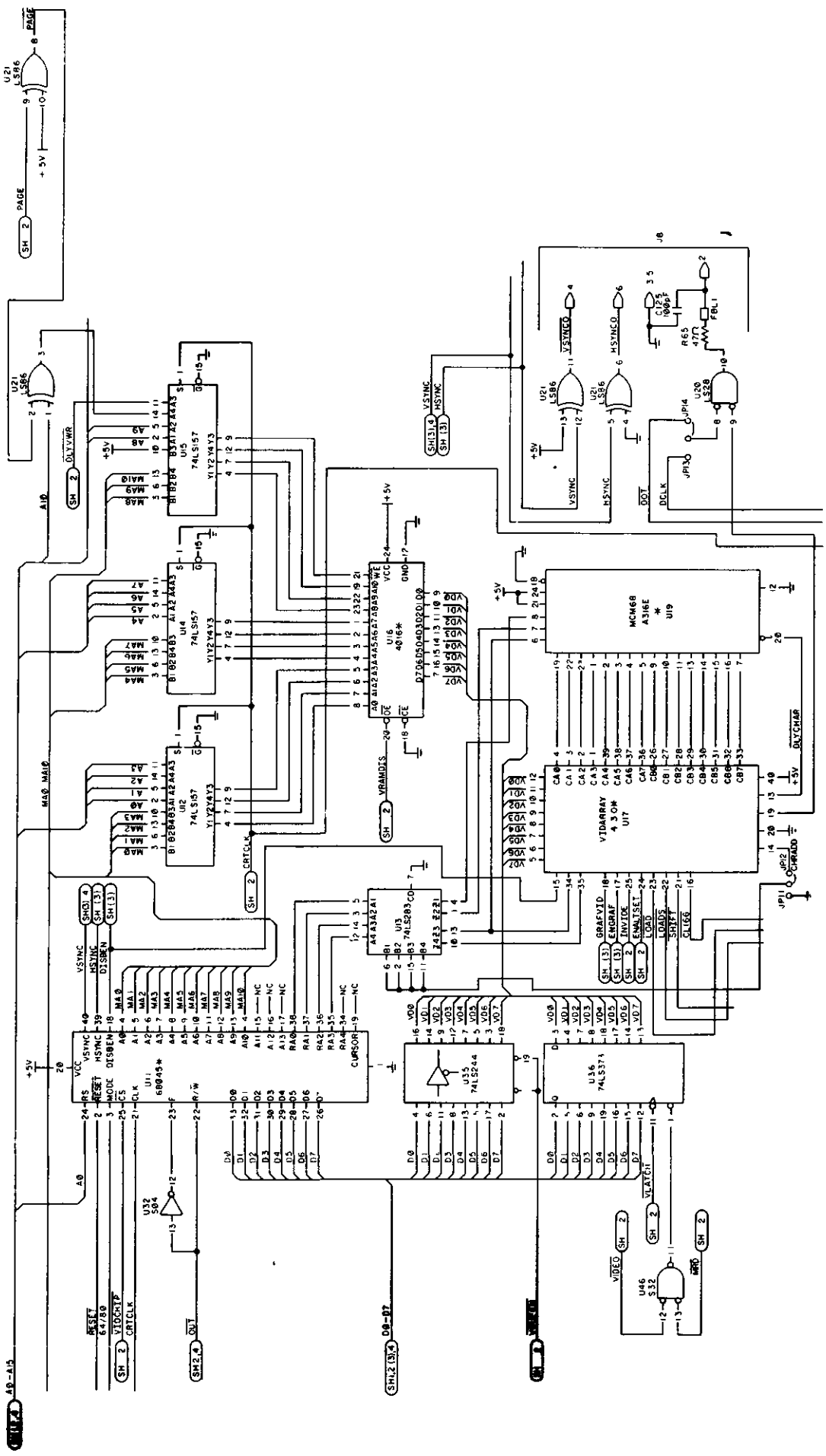


Figure 2-16. Video Circuit
(Page 3 of Schematic)

2.1.9 Keyboard

The interface to the keyboard is a matrix composed of address lines in one direction and data lines in the other. The address lines have two open collector buffers (U26 and U40) on the output to the keyboard.

The input is pulled-up with an 820 ohm resistor and is then fed into two CMOS Inputs (U55 and U56) which act as a driver on data lines.

2.1.10 Real Time Clock

The Real Time Clock circuit in the Model 4 provides a 30 Hz (in the 2 MHz CPU Mode) or 60 Hz (in the 4 MHz CPU Mode) interrupt to the CPU. By counting the number of interrupts that have occured, the CPU can keep track of the time. The 60 Hz vertical sync signal from the video circuitry is divided by two (2 MHz Mode) by U10 and the 30 Hz at pin 9 of U46 is used to generate the interrupts. In the 4 MHz mode, the signal FAST places a logic low at pin 4 of U10, causing the signal VSYNC to pass through U46 at its normal rate and trigger interrupts at the 60 Hz rate. Note that any time interrupts are disabled, the accuracy of the clock suffers.

2.1.11 Line Printer Port

The printer status lines are read by the CPU by enabling buffer U108. This buffer will be enabled for any input from port F8 or F9, or any memory read from location 37E8 or 37E9 when in the Model III mode. For a listing of bit status, refer to the bit map.

After the printer driver software determines that the printer is ready to receive a character (by reading the status), the character to be printed is output to port F8. This latches the character into U107, and simultaneously fires the one-shot U63 to provide the appropriate strobe to the printer.

2.1.12 Graphics Port

The graphics port on the Model 4 is provided to attach the optional high resolution graphics board and provides the necessary signals to interface not only to the CPU (such as data lines, address lines, address decodes, and control lines), but also the signals needed to synchronize the output of the Video Circuit and the Graphics board and control to provide features such as overlay.

Pin Number	Signature
1	D0
2	D1
3	D2
4	D3
5	D4
6	D5
7	D6
8	D7
9	GEN*
10	DCLK
11	A0
12	A1
13	A2
14	J
15	GRAPVID
16	ENGRAF
17	DISBEN
18	VSYNC
19	HSYNC
20	RESET*
21	WAIT*
22	H
23	I
24	IN*
25	GND
26	+5
27	N/C
28	CL166
29	GND
30	+5
31	GND
32	+5
33	GND
34	+5

Table 2-5

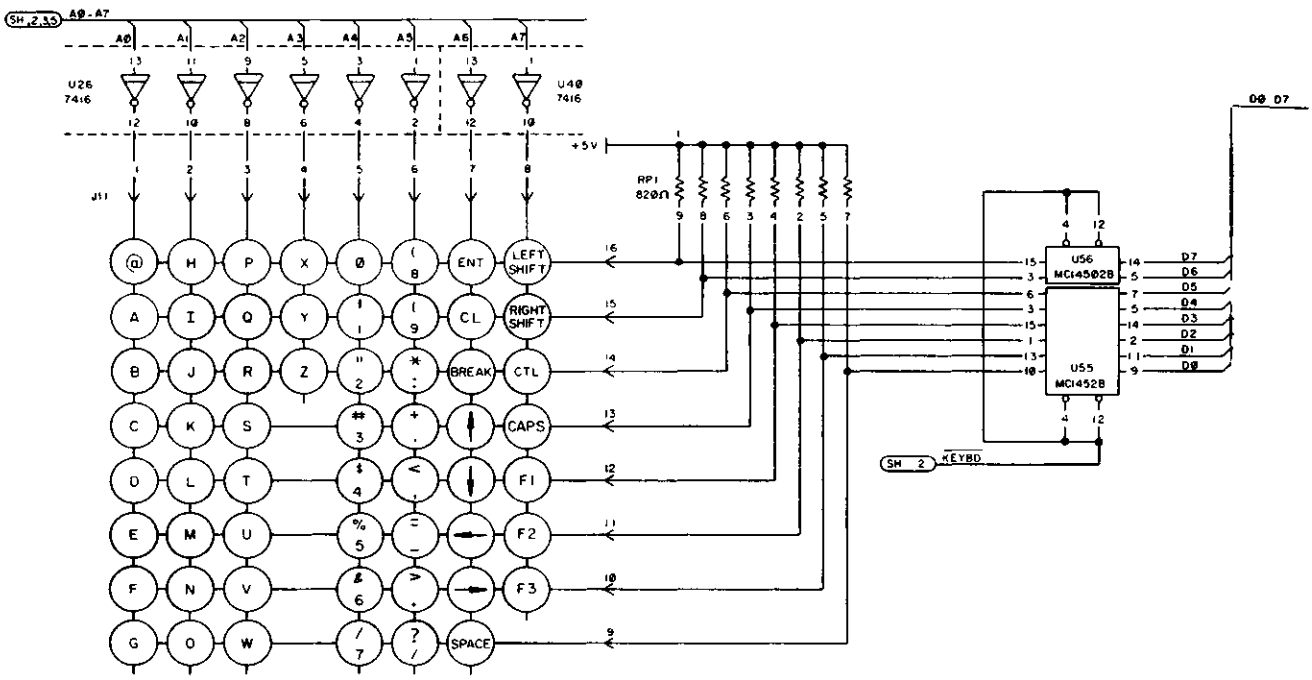


Figure 2-17. Keyboard

(Page 4 of Schematic)

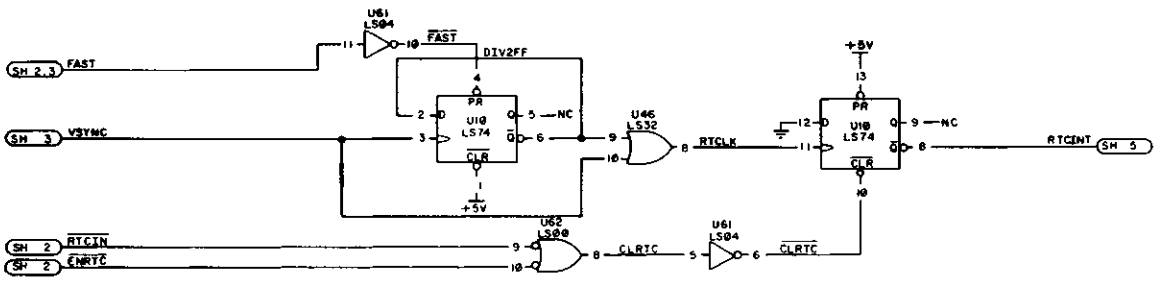


Figure 2-18. RTC

(Page 4 of Schematic)

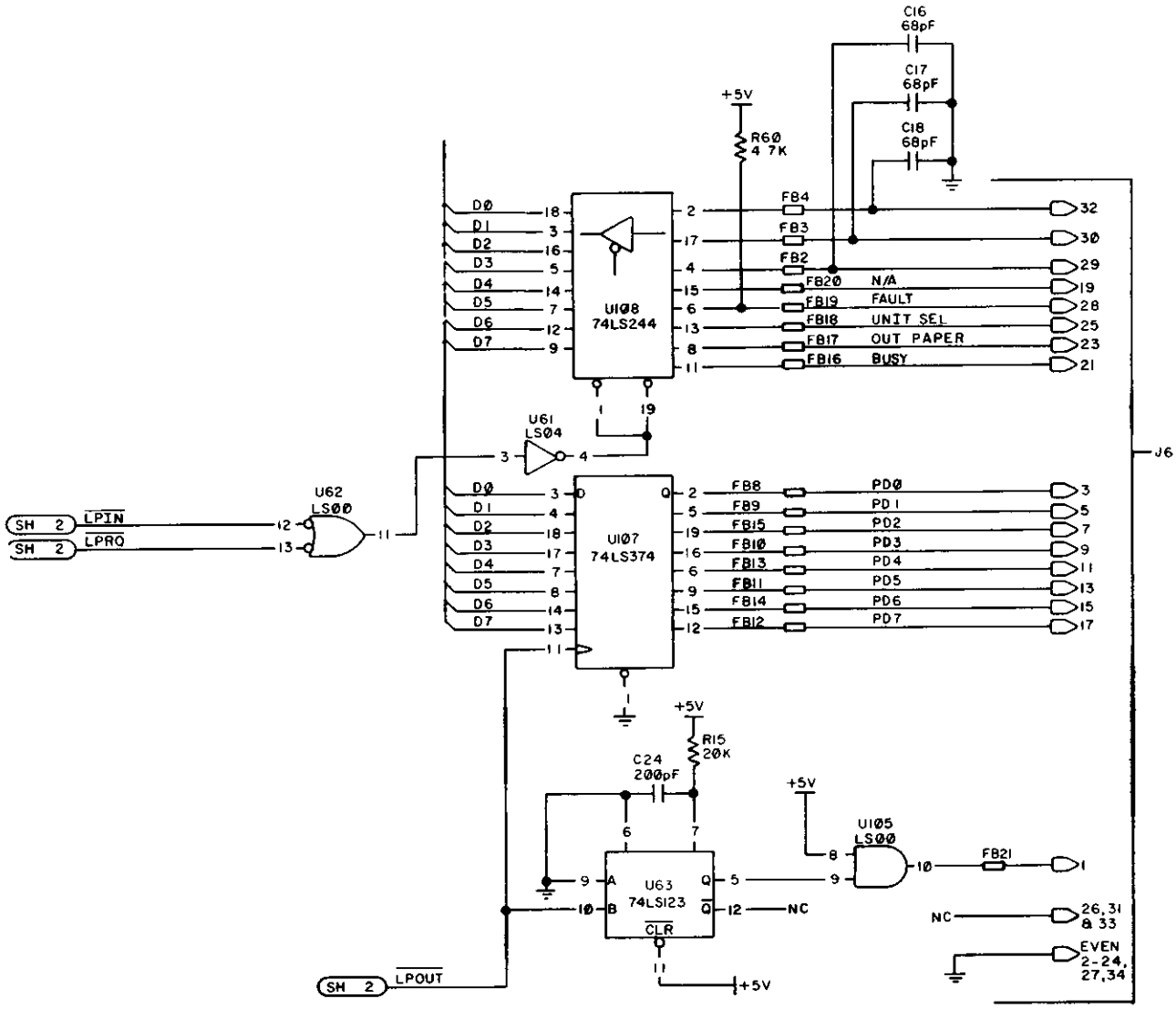


Figure 2-19. Printer Circuit

(Page 4 of Schematic)

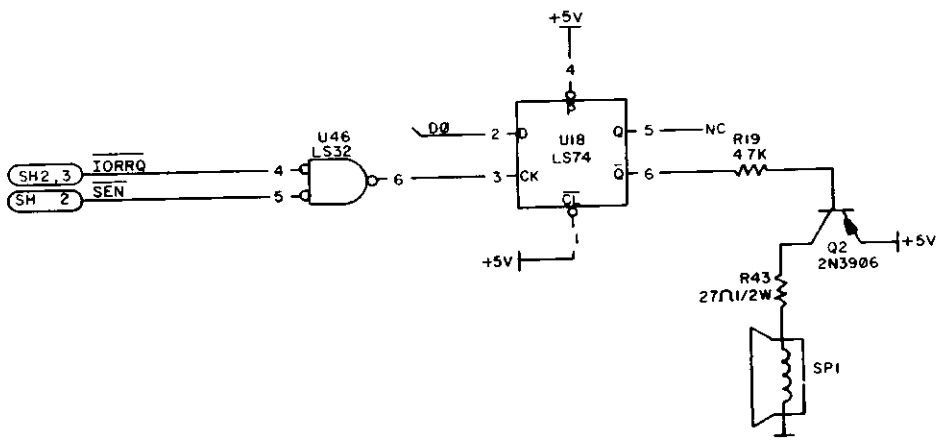


Figure 2-20. Sound

(Page 4 of Schematic)

2.1.13 Sound Port

The sound circuit is compatible with the optional sound board on the older version of the Model 4 and works in a similar fashion Sound is generated by setting and clearing data bit zero on successive OUTs to port 90H The state of D0 is latched in U18 which is amplified by Q2 to drive the speaker (SP1)

2.1.14 I/O Bus Port

The Model 4 Gate Array Bus is designed to allow easy and convenient interfacing of I/O devices to the Model 4 The I/O Bus supports all the signals necessary to implement a device compatible with the Z-80s I/O structure That is

Addresses

A0 to A7 allow selection of up to 256 input and 256 output devices if external I/O is enabled

Ports 80H to 0FFH are reserved for System use

Data

DB0 to DB7 allow transfer of 8-bit data onto the processor data bus if external I/O is enabled

Control Lines

a IN* — Z-80 signal specifying that an input is in progress Gated with IORQ

b OUT* — Z-80 signal specifying that an output is in progress Gated with IORQ

c RESET* — system reset signal

d IOBUSINT* — input to the CPU signaling an interrupt from an I/O Bus device if I/O Bus interrupts are enabled

e IOBUSWAIT* — input to the CPU wait line allowing I/O Bus device to force wait states on the Z-80 if external I/O is enabled

f EXTIOSEL* — input to CPU which switches the I/O Bus data bus transceiver and allows an INPUT instruction to read I/O Bus data

g M1* — and IORQ* — standard Z-80 signals

The address line, data line, and control lines a to c and e to g are enabled only when the ENEXIO bit is set to a one

To enable I/O interrupts, the ENIOBUSINT bit in the CPU IO-PORT E0 (output port) must be a one However even if it is disabled from generating interrupts the status of the IOBUSINT* line can still read on the appropriate bit of CPU IO-PORT E0 (input port)

See Model 4 Port Bit assignment for 0FF 0EC and 0E0

The Model 4 CPU board is fully protected from foreign I/O devices in that all the I/O bus signals are buffered and can be disabled under software control To attach and use an I/O device on the I/O Bus, certain requirements (both hardware and software) must be met

For input port device use, you must enable external I/O devices by writing to port 0ECH with bit 4 on in the user software This will enable the data bus, address lines, and control signals to the I/O Bus edge connector When the input device is selected, the hardware will acknowledge by asserting EXTIOSEL* low This switches the data bus transceiver and allows the CPU to read the contents of the I/O Bus data lines See Figure 2-21 for the timing EXTIOSEL* can be generated by NANDing IN and the I/O port address

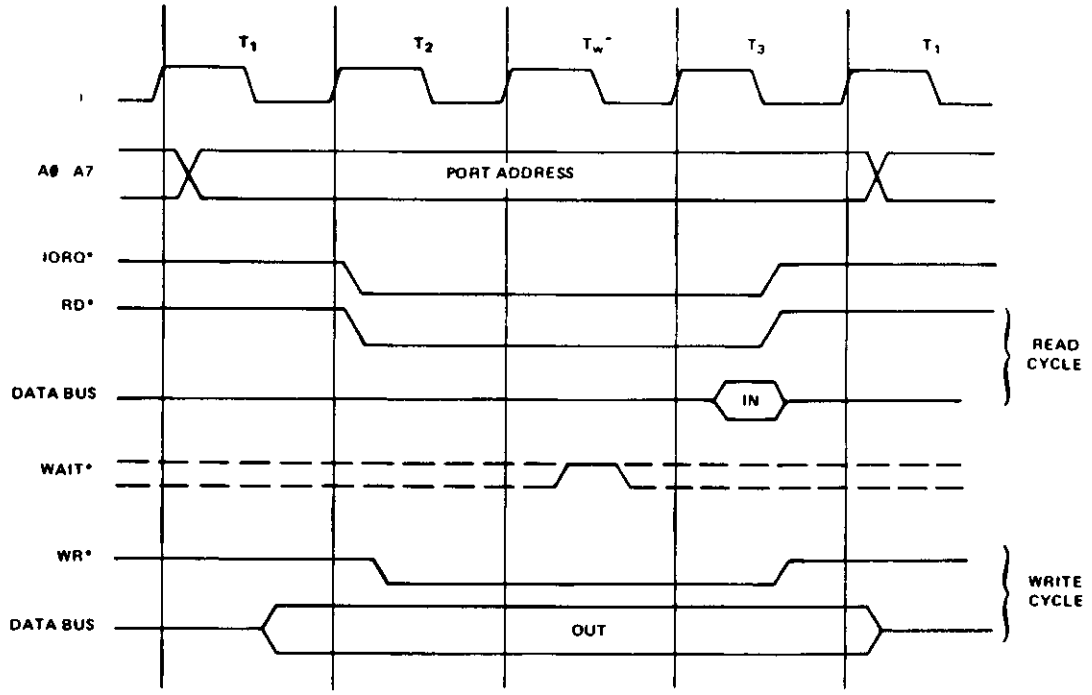
Output port device use is the same as the input port device in use, in that the external I/O devices must be enabled by writing to port 0ECH with bit 4 on in the user software — in the same fashion

For either input or output devices, the IOBUSWAIT* control line can be used in the normal way for synchronizing slow devices to the CPU Note that since dynamic memories are used in the Model 4, the wait line should be used with caution Holding the CPU in a wait state for 2 msec or more may cause loss of memory contents since refresh is inhibited during this time It is recommended that the IOBUSWAIT* line be held active no more than 500 msec with a 25% duty cycle

The Model 4 will support Z-80 mode 1 interrupts A RAM jump table is supported by the LEVEL II BASIC ROMs and the user must supply the address of his interrupt service routine by writing this address to locations 403E and 403F When an interrupt occurs, the program will be vectored to the user supplied address if I/O Bus interrupts have been enabled To enable I/O Bus interrupts, the user must set bit 3 of Port 0E0H

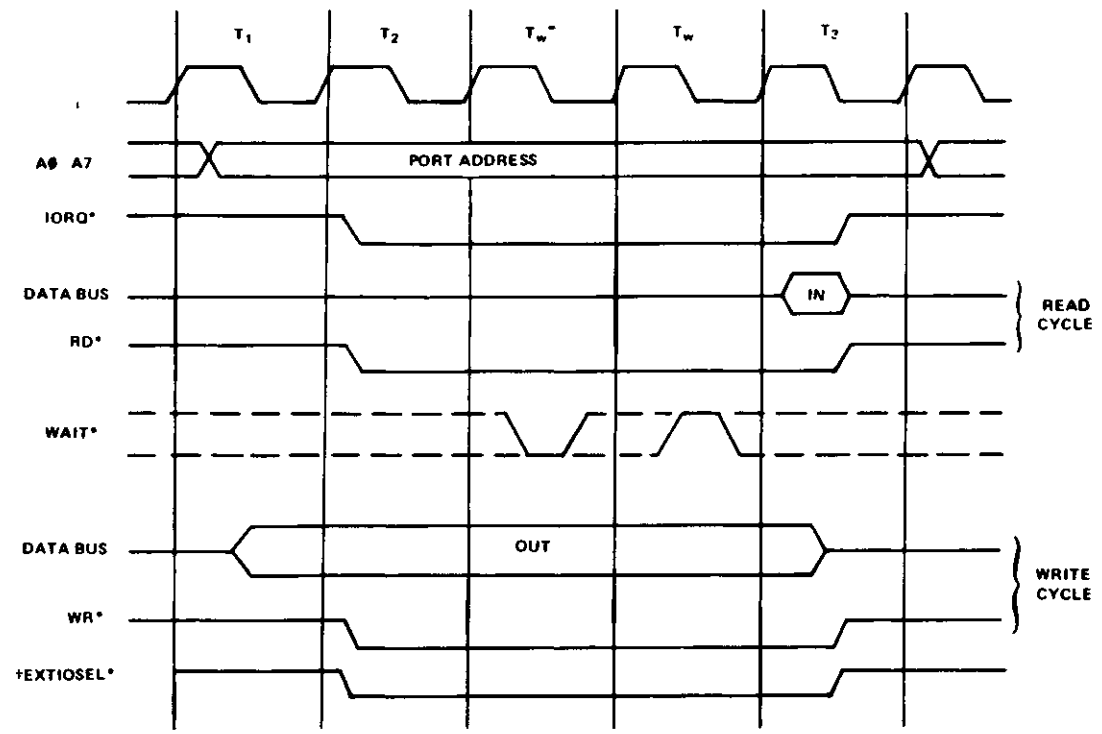
The actual implementation is shown in Figure 2-22 The data is buffered in both directions using a 74LS245 (U101) The addresses are buffered with a 74LS244 (U102) and the control lines out are buffered by a 74LS367 Note that RESET* is always enabled out, this is to power-up reset any device or clear any device before enabling the bus structure This prevents any user from tying-up the bus when enabling the port in an unknown state

Input or Output Cycles.



*Inserted by Z80 CPU

Input or Output Cycles with Wait States.



*Inserted by Z80 CPU

†Coincident with IORQ* only on INPUT cycle.

Figure 2-21. I/O BUS TIMING DIAGRAM

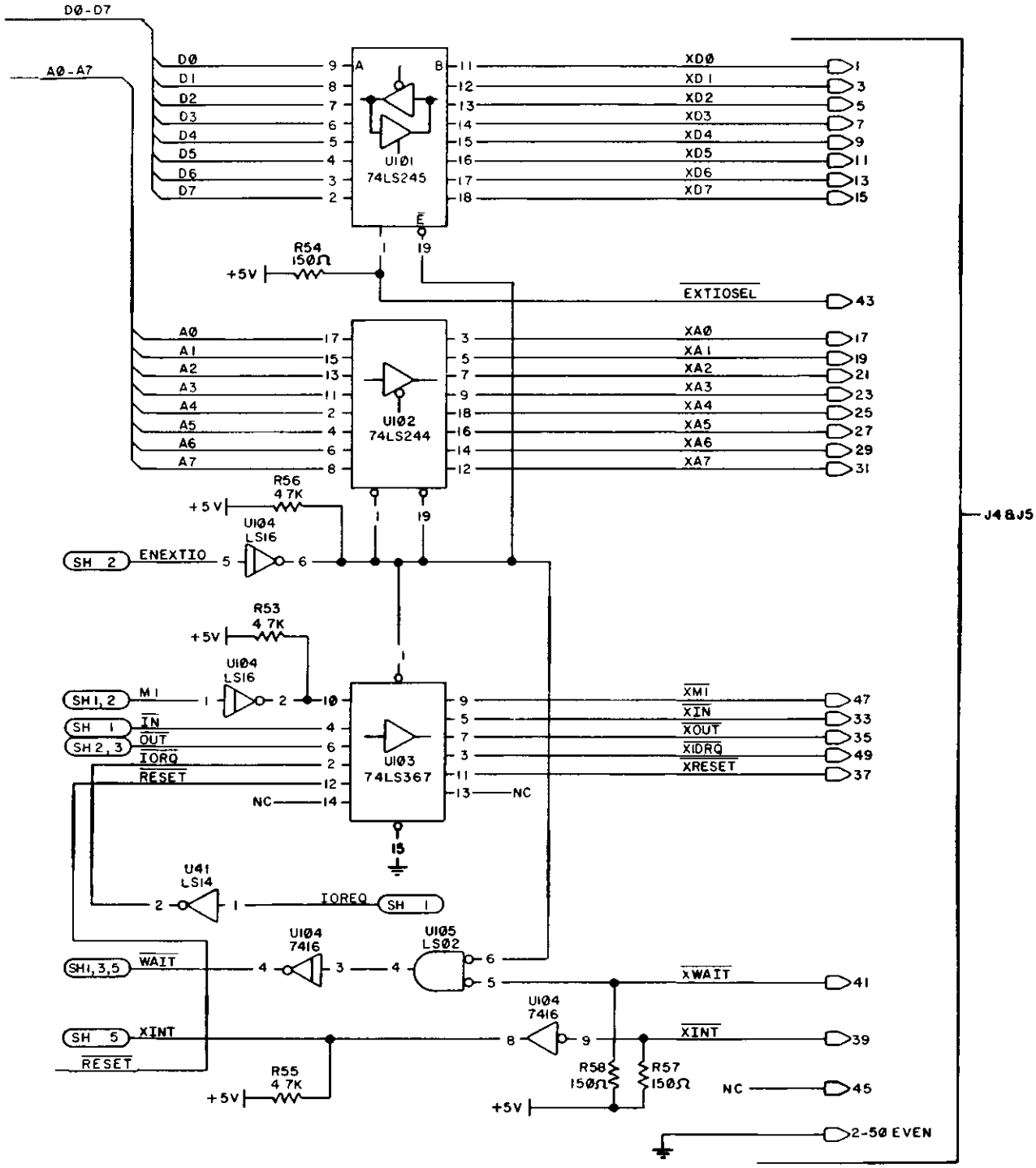


Figure 2-22. I/O Port

(Page 4 of Schematic)

Data Bit	Function
D0	Selects Drive 0 when set*
D1	Selects Drive 1 when set*
D2	Selects Drive 2 when set*
D3	Selects Drive 3 when set*
D4	Selects Side 0 when reset Selects Side 1 when set
D5	Write precompensation enabled when set disabled when reset
D6	Generates WAIT if set
D7	Selects MFM mode if set Selects FM mode if reset

*Only one of these bits should be set per output

Hex D flip-flop U79 (74L174) latches the drive select bits, side select and FM* MFM bits on the rising edge of the control signal DRVSEL* Gate Array 4 4(U76) is used to latch the Wait Enable and Write precompensation enable bits on the rising edge of DRVSEL* The rising edge of DRVSEL* also triggers a one-shot (Internal to U76) which produces a Motor On to the disk drives The duration of the Motor On signal is approximately three seconds The spindle motors are not designed for continuous operation Therefore, the inactive state of the Motor On signal is used to clear the Drive Select Latch, which de-selects any drives which were previously selected The Motor On one-shot is retriggerable by simply executing another OUT instruction to the Drive Select Latch

Wait State Generation and WAITIMOUT Logic

As previously mentioned, a wait state to the CPU can be initiated by an OUT to the Drive Select Latch with D6 set Pin 10 of U76 will go high after this operation This signal is inverted by 1/4 of U96 and is routed to the CPU where it forces the Z80A into a wait state The Z80A will remain in the wait state as long as WAIT* is low Once initiated, the WAIT* will remain low until one of five conditions is satisfied If INTRQ, DRQ, or RESET inputs become active (logic high), it causes WAIT* to go high which allows the Z80 to exit the wait state An internal timer on U70 serves as a watchdog timer to insure that a wait condition will not persist long enough to destroy dynamic RAM contents This internal watchdog timer logic will limit the duration of a wait to 1024 µsec, even if the FDC chip should fail to generate a DRQ or an INTRQ

If an OUT to Drive Select Latch is initiated with D6 reset (logic low), a WAIT is still generated The internal timer on U70 will count to 2 which will clear the WAIT state This allows the WAIT to occur only during the OUT instruction to prevent violating any Dynamic RAM parameters

NOTE This automatic WAIT will cause a 5 to 1 µsec wait each time an out to Drive Select Latch is performed

Clock Generation Logic

A 16 MHz crystal oscillator and Gate Array 4 4 (U76) are used to generate the clock signals required by the FDC board The 16 MHz oscillator is implemented internal to U76 and a quartz crystal (Y2) The output of the oscillator is divided by 2 to generate on 8 MHz clock This is used by the FDC 1773 (U75) for all internal timing and data separation U76 further divides the 16 MHz clock to drive the watchdog timer circuit

Disk Bus Output Drivers

High current open collector drivers U96, 94 and 93 are used to buffer the output signals from the FDC circuit to the disk drives

Write Precompensation and Write Data Pulse Shaping Logic

All write precompensation is generated internal to the FDC chip 1773 (U75) Write Precompensation occurs when WG goes high and write precompensation is enabled from the software ENP is multiplexed with RDY and is controlled by WG at pin 20 of U75 Write data is output on pin 22 of U75 and is shaped by a one-shot (1/2 of U98) which stretches the data pulses to approximately 500 nsec

Clock and Read Data Recovery Logic

The Clock and Read Data Recovery Logic is done internal to the 1773 (U75)

Floppy Disk Controller Chip

The 1773 is an MOS LSI device which performs the functions of a floppy disk formatter/controller in a single chip implementation. The following port addresses are assigned to the internal registers of the 1773 FDC chip:

Port No.	Function
F0H	Command/Status Register
F1H	Track Register
F2H	Sector Register
F3H	Data Register

2.1.15 Cassette Circuit

The cassette write circuitry latches the two LSBs (D0 and D1) for any output to port FF (hex) The outputs of these latches (U51) are then resistor summed to provide three discrete voltage levels (500 Baud only) The firmware toggles the bits to provide an output signal of the desired frequency at the summing node

There are two types of cassette Read circuits — 500 baud and 1500 baud The 500 baud circuit is compatible with both Model I and III The input signal is amplified and filtered by Op amps (U23 and U54) Part of U22 then forms a Zero Crossing Detector, the output of which sets the latch U37 A read of Port FF enables buffer U52 which allows the CPU to determine whether the latch has been set, and simultaneously resets the latch The firmware determines by the timing between settings of the latch whether a logic "'one" or "'zero" was read in from the tape

The 1500 baud cassette read circuit is compatible with the Model III cassette system The incoming signal is compared to a threshold by part of U22 U22's output will then be either high or low and clock about one-half of U37, depending on whether it is a rising edge or a falling edge If interrupts are enabled, the setting of either latch will generate an interrupt As in the 500 baud circuit, the firmware decodes the interrupts into the appropriate data.

For any cassette read or write operation, the cassette relay must be closed in order to start the motor of the cassette deck A write to port EC hex with bit one set will latch U53, which turns on transistor Q3 and energizes the relay K1 A subsequent write to this port with bit one clear will clear the latch and de-energize the relay

2.1.16 FDC Circuit

The TRS-80 Model 4 Floppy Disk Interface provides a standard 5-1/4" floppy disk controller The Floppy Disk Interface supports single and double density encoding schemes Write precompensation can be software enabled or disabled beginning at any track, although the system software enables write precompensation for all tracks greater than twenty-one The amount of write precompensation is 125 nsec and is not adjustable One to four drives may be controlled by the interface All data transfers are accomplished by CPU data requests In double density operation, data transfers are synchronized to the CPU by forcing a wait to the CPU and clearing the wait by a data request from the FDC chip The end of the data transfer is indicated by generation of a non-maskable interrupt from the interrupt request output of the FDC chip A hardware watchdog timer insures that any error condition will not hang the wait line to the CPU for a period long enough to destroy RAM contents

Control and Data Buffering

The Floppy Controller is an I/O port-mapped device which utilizes ports E4H, F0H, F1H, F2H, F3H, and F4H The decoding logic is implemented in the Address Decoding (for more information see Port Map) U78 is a bi-directional, 8-bit transceiver used to buffer data to and from the FDC and RS-232 circuits The direction of data transfer is controlled by the combination of control signals DISKIN*, RDINTSTATUS*, RDNINSTATUS*, and RS232IN* If any signal is active (logic low), U78 is enabled to drive data onto the CPU data bus If all signals are inactive (logic high), U78 is enabled to receive data from the CPU board data bus A second buffer U77 is used to buffer the FDC chip data to the FDC/RS232 Data Bus, (BD0-BD7) U77 is enabled by Chip Select and its direction controlled by DISKIN* Again, if DISKIN* is active (logic low), data is enabled to drive from the FDC chip to the Main Data Busses If DISKIN* is inactive (logic high), data is enabled to be transferred to the FDC chip

Non-maskable Interrupt Logic

Gate Array 4 4 (U75) is used to latch data bits D6 and D7 on the rising edge of the control signal WRNMIMASKREG* This enables the conditions which will generate a non-maskable interrupt to the CPU The NMI interrupt conditions which are programmed by doing an OUT instruction to port E4H with the appropriate bits set If data bit 7 is set, an FDC interrupt is enabled to generate an NMI interrupt If data bit 7 is reset, interrupt requests from the FDC are disabled If data bit 6 is set, a Motor Time Out is enabled to generate an NMI interrupt If data bit 6 is reset, interrupts on Motor Time Out are disabled An IN instruction from port E4H enables the CPU to determine the course of the non-maskable interrupt Data bit 7 indicates the status of FDC interrupt request (INTRQ) (0 = true, 1 = false) Data bit 6 indicates the status of Motor Time Out (0 = true, 1 = false) Data bit 5 indicates the status of the Reset signal (0 = true, 1 = false) The control signal RDNMISTATUS* gates this status onto the CPU data bus when active (logic low)

Drive Select Latch and Motor ON Logic

Selecting a drive prior to disk I/O operation is accomplished by doing an OUT instruction to port F4H with the proper bit set The following table describes the bit allocation of the Drive Select Latch

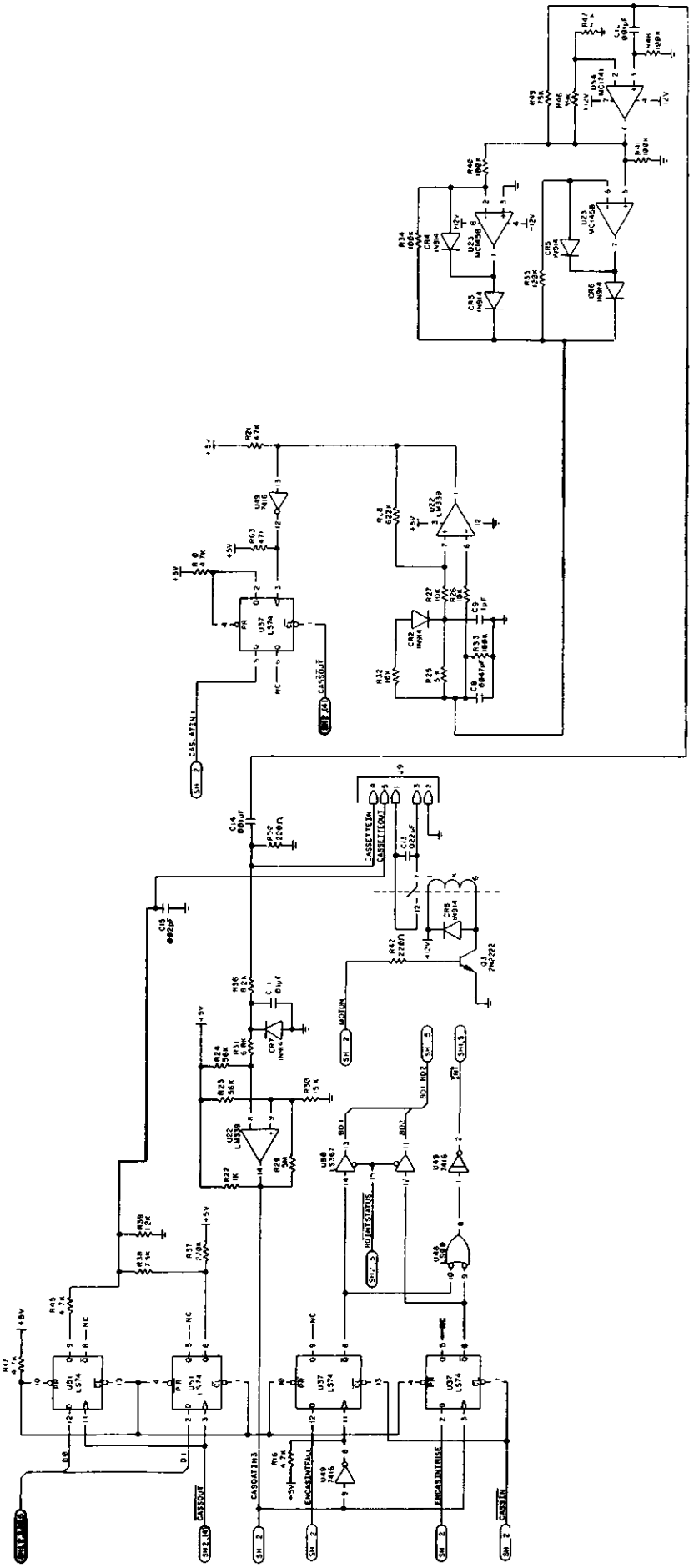


Figure 2-23. Circuit Cassette
(Page 4 of Schematic)

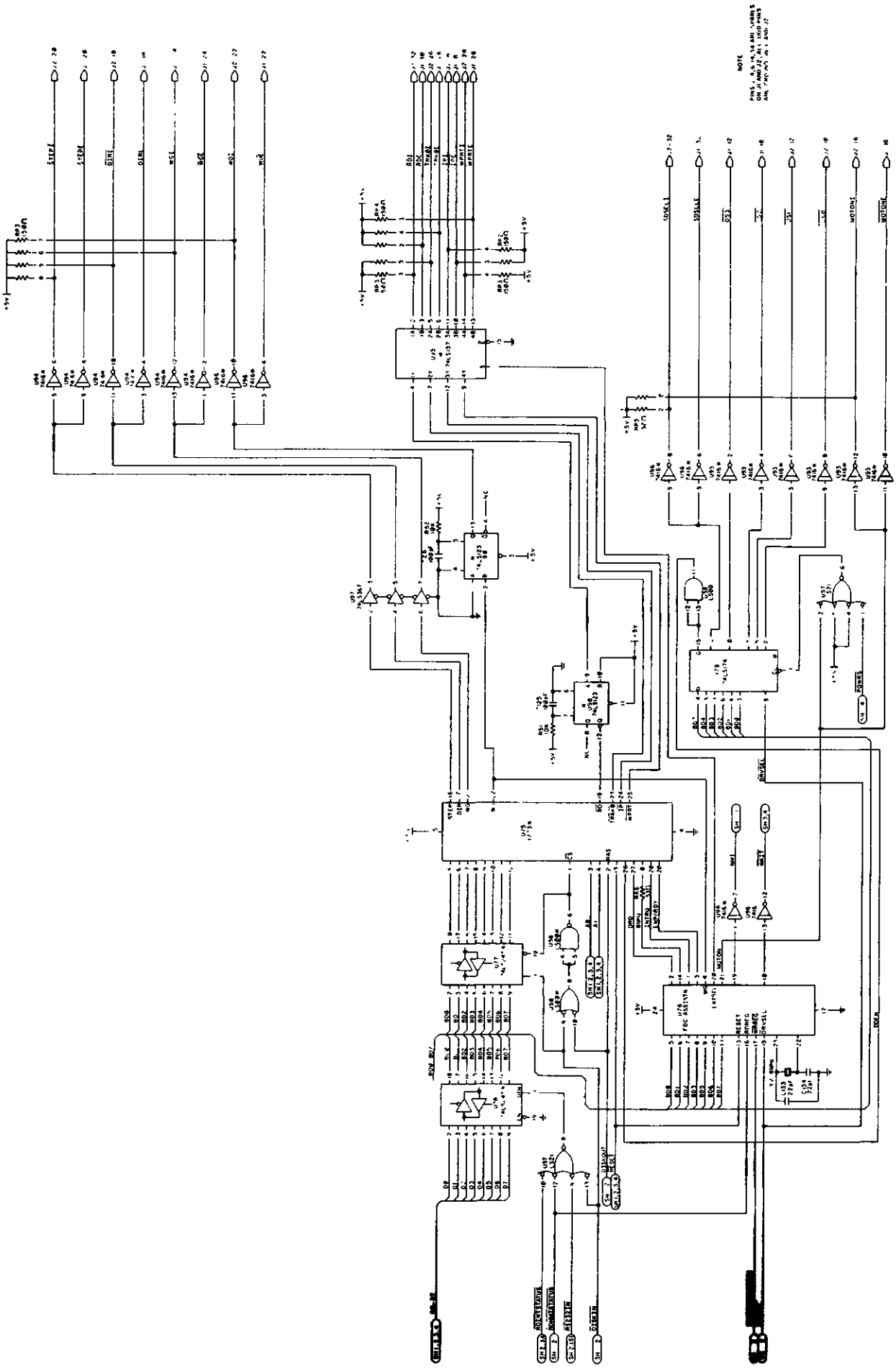


Figure 2-24. F.D.C. Circuit
(Page 5 of Schematic)

2.1.17 RS-232C Circuit

RS-232C Technical Description

The RS-232C circuit for the Model 4 computer supports asynchronous serial transmissions and conforms to the EIA RS-232C standards at the input-output interface connector (J3) The heart of the circuit is the TR1865 Asynchronous Receiver/Transmitter U84 It performs the job of converting the parallel byte data from the CPU to a serial data stream including start, stop, and parity bits For a more detailed description of how this LSI circuit performs these functions, refer to the TR1865 data sheets and application notes The transmit and receive clock rates that the TR1865 needs are supplied by the Baud Rate Generator U104 This circuit takes the 5 0688 MHz supplied by the system timing circuit and the programmed information received from the CPU over the data bus and divides the basic clock rate to provide two clocks The rates available from the BRG go from 50 Baud to 19200 Baud See the BRG table for the complete list.

Interrupts are supported in the RS-232C Circuit by the Interrupt mask register and the Status register internal to Gate Array 4 5 (U82) The CPU looks here to see which kind of interrupt has occurred Interrupts can be generated on receiver data register full, transmitter register empty, and any one of the errors — parity, framing, or data overrun This allows a minimum of CPU overhead in transferring data to or from the UART The interrupt mask register is port E0 (write) and the interrupt status register is port E0 (read) Refer to the IO Port description for a full breakdown of all interrupts and their bit positions

All Model I, III, and 4 software written for the RS-232C interface is compatible with the Model 4 Gate Array RS-232C circuit, provided the software does not use the sense switches to configure the interface The programmer can get around this problem by directly programming the BRG and UART for the desired configuration or by using the SETCOM command of the disk operating system to configure the interface The TRS-80 RS-232C Interface hardware manual has a good discussion of the RS-232C standard and specific programming examples (Catalog Number 26-1145)

BRG Programming Table

Nibble Loaded	Transmit/ Receive Baud Rate	16X Clock	Suported by SETCOM
0H	50	0.8 kHz	Yes
1H	75	1.2 kHz	Yes
2H	110	1.76 kHz	Yes
3H	134.5	2 1523 kHz	Yes
4H	150	2.4 kHz	Yes
5H	300	4.8 kHz	Yes
6H	600	9.6 kHz	Yes
7H	1200	19 2 kHz	Yes
8H	1800	28.8 kHz	Yes
9H	2000	32.081 kHz	Yes
AH	2400	38.4 kHz	Yes
BH	3600	57.6 kHz	Yes
CH	4800	76.8 kHz	Yes
DH	7200	115.2 kHz	Yes
EH	9600	153.6 kHz	Yes
FH	19200	307.2 kHz	Yes

Pinout Listing

The RS-232C circuit is port mapped and the ports used are E8 to EB Following is a description of each port on both input and output.

Port	Input	Output
E8	Modem status	Master Reset, enables UART control register load
EA	UART status	UART control register load and modem control
E9	Not Used	Baud rate register load enable bit
EB	Receiver Holding register	Transmitter Holding register

The following list is a pinout description of the DB-25 connector (P1)

Pin No.	Signal
1	PGND (Protective Ground)
2	TD (Transmit Data)
3	RD (Receive Data)
4	RTS (Request to Send)
5	CTS (Clear To Send)
6	DSR (Data Set Ready)
7	SGND (Signal Ground)
8	CD (Carrier Detect)
19	SRTS (Spare Request to Send)
20	DTR (Data Terminal Ready)
22	RI (Ring Indicate)

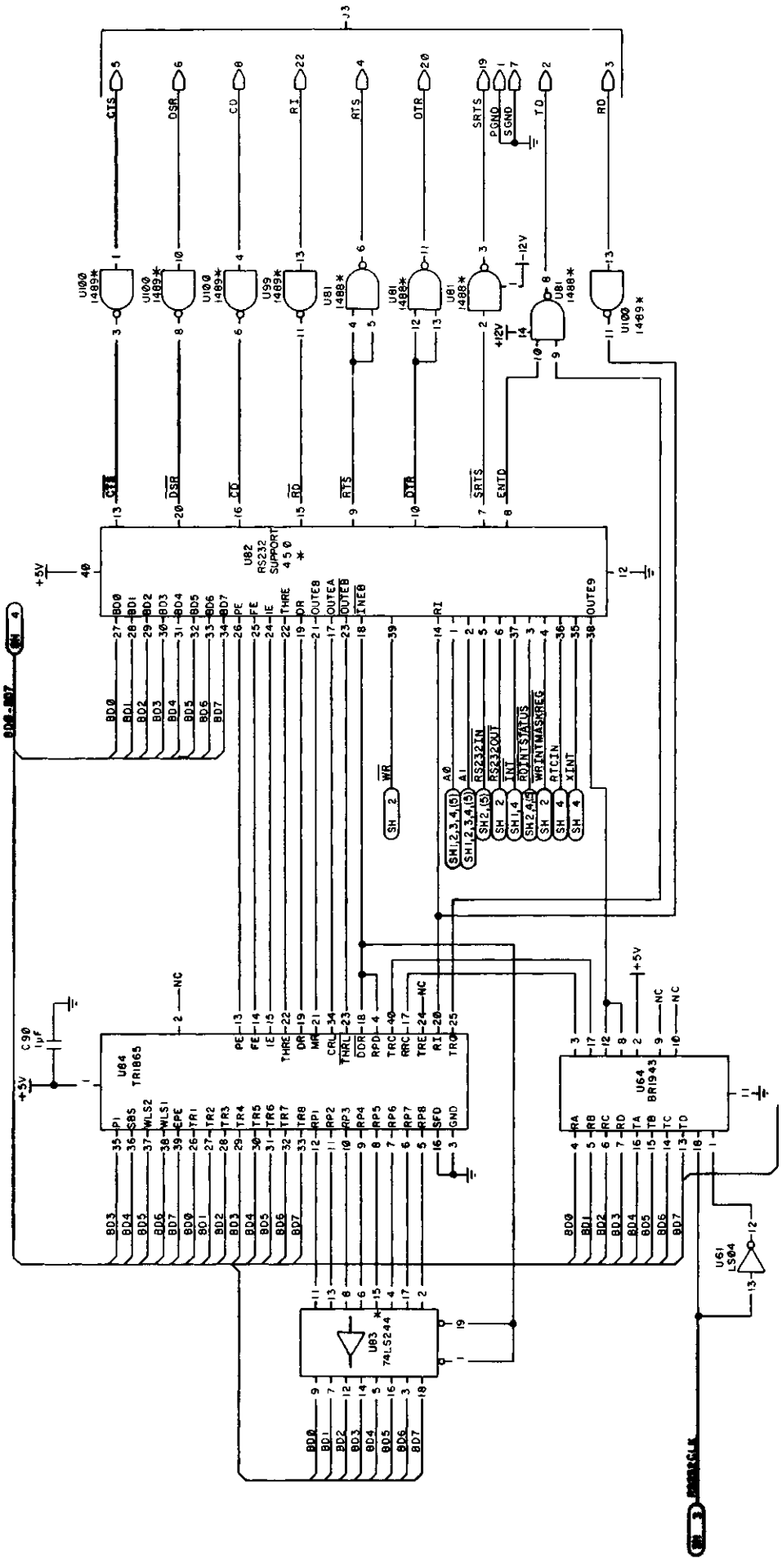


Figure 2-25. RS232C Circuit

(Page 5 of Schematic)

Model 4 Gate Array
I/O Pin Assignments

J1		J2		J3		J4		J5	
Pin No.	**Signal**	**Pin No.**	**Signal**	**Pin No.**	**Signal**	**Pin No.**	**Signal**	**Pin No.**	**Signal**
1.	GND	1.	GND	1.	PGND	1.	XDO	1.	XDO
2.		2.		2.	TD	2.	GND	2.	GND
3.	GND	3.	GND	3.	RD	3.	XD1	3.	XD1
4.		4.		4.	RTS	4.	GND	4.	GND
5.	GND	5.	GND	5.	CTS	5.	XD2	5.	XD2
6.		6.		6.	DSR	6.	GND	6.	GND
7.	GND	7.	GND	7.	SGND	7.	XD3	7.	XD3
8.	IPE*	8.	IPI*	8.	CD	8.	GND	8.	GND
9.	GND	9.	GND	9.		9.	XD4	9.	XD4
10.	DS2*	10.	DS0*	10.		10.	GND	10.	GND
11.	GND	11.	GND	11.		11.	XD5	11.	XD5
12.	DS3*	12.	DS1*	12.		12.	GND	12.	GND
13.	GND	13.	GND	13.		13.	XD6	13.	XD6
14.		14.		14.		14.	GND	14.	GND
15.	GND	15.	GND	15.		15.	XD7	15.	XD7
16.	MOTNE*	16.	MOTONI*	16.		16.	GND	16.	GND
17.	GND	17.	GND	17.		17.	XA0	17.	XA0
18.	DIRE*	18.	DIRI*	18.		18.	GND	18.	GND
19.	GND	19.	GND	19.	SRTS	19.	XA1	19.	XA1
20.	STEPE*	20.	STEPI*	20.	DTR	20.	GND	20.	GND
21.	GND	21.	GND	21.		21.	XA2	21.	XA2
22.	WDE*	22.	WDI*	22.	RI	22.	GND	22.	GND
23.	GND	23.	GND	23.		23.	XA3	23.	XA3
24.	WGE*	24.	WGI*	24.		24.	GND	24.	GND
25.	GND	25.	GND	25.		25.	XA4	25.	XA4
26.	TRK0E*	26.	TRK0I*	26.		26.	GND	26.	GND
27.	GND	27.	GND	27.		27.	XA5	27.	XA5
28.	WPRTE*	28.	WPRTI*	28.		28.	GND	28.	GND
29.	GND	29.	GND	29.		29.	XA6	29.	XA6
30.	RDE*	30.	RDI*	30.		30.	GND	30.	GND
31.	GND	31.	GND	31.		31.	XA7	31.	XA7
32.	SDSELE	32.	SDSELI	32.		32.	GND	32.	GND
33.	GND	33.	GND	33.		33.	XIN*	33.	XIN*
34.		34.		34.		34.	GND	34.	GND
						35.	XOUT*	35.	XOUT*
						36.	GND	36.	GND
						37.	XRESET*	37.	XRESET*
						38.	GND	38.	GND
						39.	XINT*	39.	XINT*
						40.	GND	40.	GND
						41.	XWAIT*	41.	XWAIT*
						42.	GND	42.	GND
						43.	EXTIO-	43.	EXTIO-
						44.	SEL*	44.	SEL*
						45.	GND	45.	GND
						46.	NC	46.	NC
						47.	GND	47.	GND
						48.	XMI*	48.	XMI0
						49.	GND	49.	GND
						50.	XIDRQ*	50.	XIDRQ*
							GND		GND

Model 4 Gate Array
I/O Pin Assignments

J6		J8		J9		J12	
Pin No.	**Signal**	**Pin No.**	**Signal**	**Pin No.**	**Signal**	**Pin No.**	**Signal**
1.		1.		1.		1.	D0
2.	GND	2.		2.	GND	2.	D1
3.	PD0	3.		3.		3.	D2
4.	GND	4.	VSYNCO*	4.	CASSETTE-	4.	D3
5.	PD1	5.		5.	IN	5.	D4
6.	GND	6.	HSYNCO	6.	CASSETTE-	6	D5
7.	PD2	7.		7.	OUT	7.	D6
8.	GND	8.		8.		8.	D7
9.	PD3	9.		9.		9.	GEN*
10.	GND	10.		10.		10.	DCLK
11.	PD4	11.		11.		11.	A0
12.	GND	12.		12.		12.	A1
13.	PD5	13.		13.		13.	A2
14.	GND	14.		14.		14.	J
15.	PD6	15.		15.		15.	GRAPVID
16.	GND	16.		16.		16.	ENGRAF
17.	PD7	17.		17.		17.	DISBEN
18.	GND	18.		18.		18.	VSYNC
19.	N/A	19.		19.		19.	HSYNC
20.	GND	20.		20.		20.	RESET*
21.	BUSY	21.		21.		21.	WAIT*
22.	GND	22.		22.		22.	H
23.	OUT PAPER	23.		23.		23.	I
24.	GND	24.		24.		24.	IN*
25.	UNIT SEL					25.	GND
26.	NC					26.	+5V
27.	GND					27.	
28.	FAULT					28.	CL166
29.						29.	GND
30.						30.	+5V
31.	NC					31.	GND
32.						32.	+5V
33.	NC					33.	GND
34.	GND					34.	+5V

SECTION III

4P THEORY OF OPERATION

3.1 MODEL 4P THEORY OF OPERATION

3.1.1 Introduction

Contained in the following paragraphs is a description of the component parts of the Model 4P CPU It is divided into the logical operational functions of the computer All components are located on the Main CPU board inside the case housing Refer to Section 3 for disassembly assembly procedures

3.1.2 Reset Circuit

The Model 4P reset circuit provides the neccessary reset pulses to all circuits during power up and reset operations R25 and C218 provide a time constant which holds the input of U121 low during power-up This allows power to be stable to all circuits before the RESET* and RESET signals are applied When C218 charges to a logic high the output of U121 triggers the input of a retriggerable one-shot multivibrator (U1) U1 outputs a pulse with an approximate width of 70 microsecs When the reset switch is pressed on the front panel this discharges C218 and holds the input of U121 low until the switch is released On release of the switch, C218 again charges up triggering U121 and U1 to reset the microcomputer

3.1.3 CPU

The central processing unit (CPU) of the Model 4P microcomputer is a Z80A microprocessor The Z80A is capable of running in either 2 MHz or 4 MHz mode The CPU controls all functions of the microcomputer through use of its address lines (A0-A15), data lines (D0-D7) and control lines (M1 IOREQ RD, WR, MREQ, and RFSH) The address lines (A0-A15) are buffered to other ICs through two 74LS244s (U68 and U26) which are enabled all the time with their enables pulled to GND The control lines are buffered to other ICs through a 74F04 (U86) The data lines (D0-D7) are buffered through a bi-directional 74LS245 (U71) which is enabled by BUSEN* and the direction is controlled by BUSDIR*

3.1.4 System Timing

The main timing reference of the microcomputer with the exception of the FDC circuit, comes from a 20 2752 MHz Crystal Oscillator (Y1) This reference is divided and used for generating all necessary timing for the CPU video circuit and RS-232-C circuit The output of the crystal oscillator is filtered by a ferritte bead (FB5) 470 ohm resistor (R46) and a 68 pf capacitor (C242) After being filtered it is fed into U126 a 16R6A PAL (Programmable Array Logic) where it is divided by 2 to generate a 10 1376 MHz signal (10M) for the 64 X 16 video display U126 divides the 20 2752 MHz by 4 to generate a 5 0688 MHz signal (RS232CLK) for the baud rate generator in the RS-232-C circuit The CPU clock is also generated by U126 which can be either 2 or 4 MHz depending on the state of FAST input (pin 9 of U126) If FAST is a logic low the 20 2752 MHz is divided by 10 which generates a 2 2752 MHz signal If FAST is a logic high the 20 2752 MHz is divided by 5 which generates a 4 05504 MHz signal The CPU clock (PCLK) is fed through an active pull-up circuit which generates a full 5-volt swing with fast rise and fall times required by the Z80A U126 the 16R6A PAL, generates all symmetrical output signals and also does not allow the PCLK output to short cycle or generate a low or high pulse under 110 nanoseconds which the Z80A also requires Refer to System Timing Fig. 3-2.

3.1.4.1 Video Timing

The video timing is controlled by a 10L8 PAL (U127) and a four-bit synchronous counter U128 (74LS161) These two ICs generate all the necessary timing signals for the four video modes 64 x 16 32 x 16, 80 x 24 and 40 x 24 Two reference clock signals are required for the four video modes One reference clock, the 10 1376 MHz signal (10M) is generated by U126 and is used by the 64 x 16 and 32 x 16 modes The second reference clock is a 12 672 MHz (12M) signal which is generated by a Phase Locked Loop (PLL) circuit and is used by the 80 x 24 and 40 x 24 modes The PLL circuit consists of U147 (74LS93), U148 (NE564 PLL), and U149 (74LS90) The original 20 2752 MHz clock is divided by 16 through U147 which generates a 1 2672 MHz signal The output of U147 is reduced in amplitude by the voltage divider network R27 and R28 and the output is coupled to the reference input of U148 by C227

The PLL (NE564) is adjusted to oscillate at 12 672 MHz by the tuning capacitor C231 This 12 672 MHz clock is then divided by 10 through U149 to generate a second 1 2672 MHz signal which is fed to a second input of U148 The two 1 2672 MHz signals are compared internally to the PLL where it corrects the 12 672 MHz output so it is synchronized with the 20 2752 MHz clock

MODSEL and 8064* signals are used to select the desired video mode 8064* controls which reference clock is used by U127 and MODSEL controls the single or double character width mode Refer to the following chart for selecting each video mode

8064*	MODSEL	Video Mode
0	0	64 x 16
0	1	32 x 16
1	0	80 x 24
1	1	40 x 24

*This is the state to be written to latch U89 Signal is inverted before being input to U127

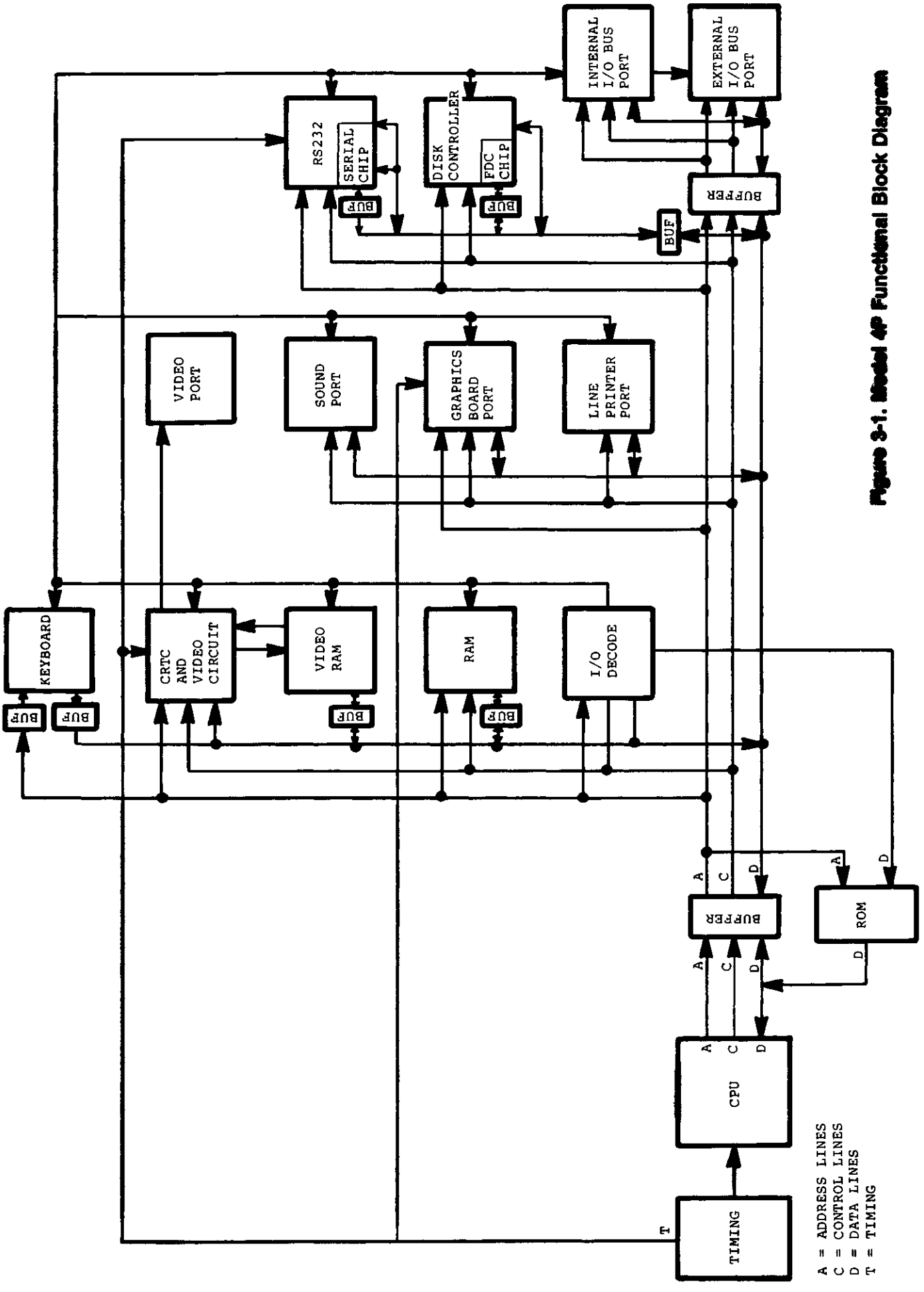


Figure 3-1. Model 4P Functional Block Diagram

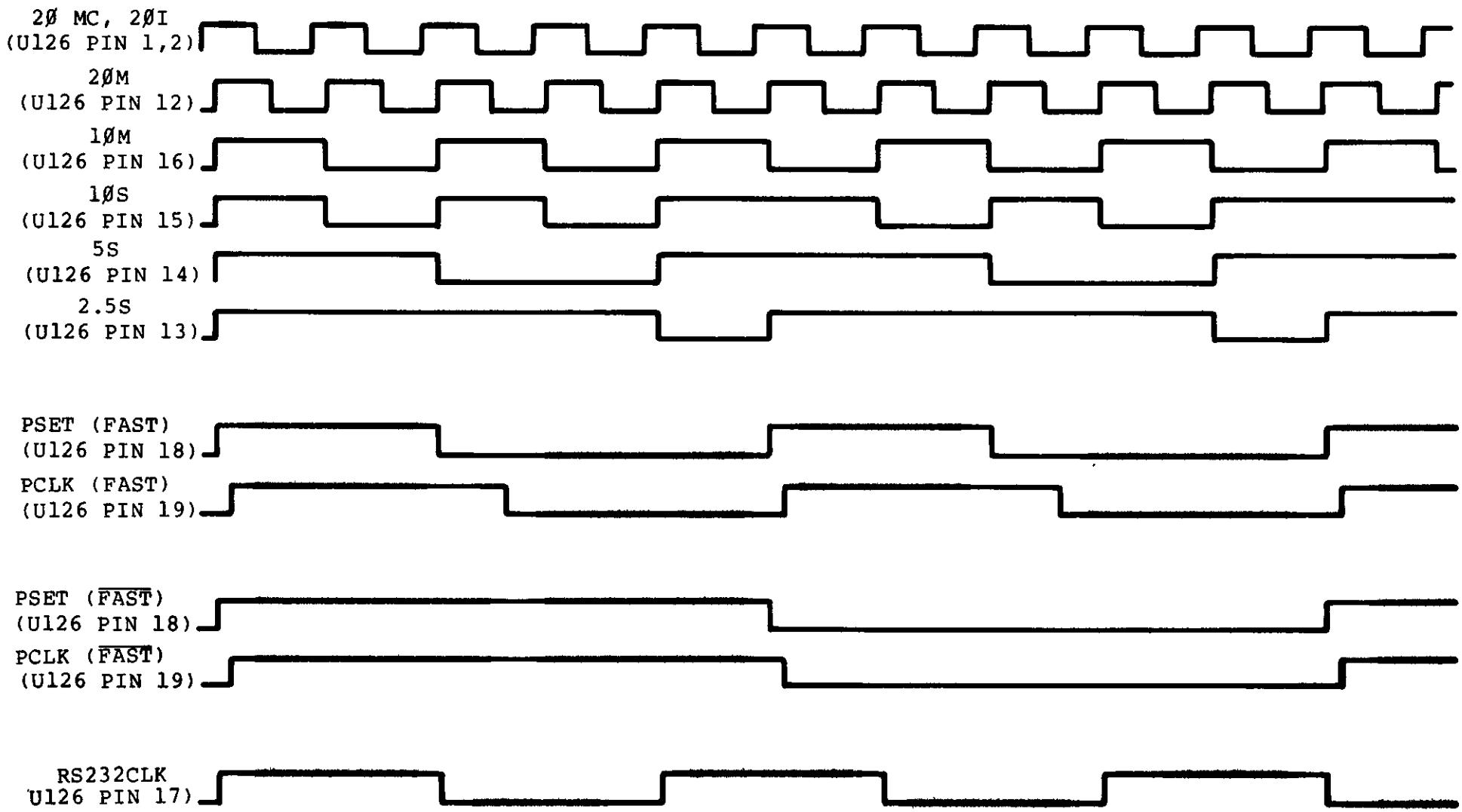


Figure 3-2. System Timing

DCLK, the reference clock selected, is output from U127. DCLK is fed back into U127 for internal timing reference and is also fed to the clock input of U128 (74LS161). U128 is configured to preload with a count of 9 each time it reaches a count of 0. This generates a signal output of TC (128 pin 15) that occurs at the start of every character time of video output. TC is used to generate LOADS* (Load Shift Register). QA and QC of U128 are used to generate SHIFT*, XADR7*, CRTCLK and LOAD* for proper timing for the four video modes. QA, QB, and QC which are referred to as H, I, and J are fed to the Graphics Port J7 for reference timings of Hires graphics video. Refer to Video Timing, Figs. 3-3 and 3-4 for timing reference.

3.1.5 Address Decode

The Address Decode section will be divided into two subsections: Memory Map decoding and Port Map decoding.

3.1.5.1 Memory Map Decoding

Memory Map Decoding is accomplished by a 16L8 PAL (U109) Four memory map modes are available which are compatible with the Model III and Model 4 microcomputers A second 16L8 PAL (U110) is used in conjunction with U109 for the memory map control which also controls page mapping of the 32K RAM pages. Refer to Memory Maps below.

3.1.5.2 Port Map Decoding

Port Map Decoding is accomplished by three 74LS138s (U87, U88, and U107). These ICs decode the low order address (A0-A7) from the CPU and decode the port being selected The IN* signal from U108 enables U87 which allows the CPU to read from a selected port and the OUT* signal, also from U108, enables U88 which allows the CPU to write to the selected port U107 only decodes the address and the IN* and OUT* signals are ANDed with the generated signals.

3.1.6 ROM

The Model 4P contains only a 4K x 8 Boot ROM (U70). This ROM is used only to boot up a Disk Operating System into the RAM memory. If Model III operation or DOS is required, then the RAM from location 0000-37FFH must be loaded with an image of the Model III or 4 ROM code and then executed. A file called MODEL A/III is supplied with the Model 4P which contains the ROM image for proper Model III operation. On power-up, the Boot ROM is selected and mapped into location 0000-0FFFH. After the Boot Sector or the ROM Image is loaded, the Boot ROM must be mapped out by OUTing to port 9CH with D0 set or by selecting Memory Map modes 2 or 3. In Mode 1 the RAM is write enabled for the full 14K. This allows the RAM area mapped where Boot ROM is located to be written to while executing out of the Boot ROM. Refer to Memory Maps.

The Model 4P Boot ROM contains all the code necessary to initialize hardware detect options selected from the keyboard read a sector from a hard disk or floppy and load a copy of the Model III ROM Image (as mentioned) into the lower 14K of RAM

The firmware is divided into the following routines

- Hardware Initialization
- Keyboard Scanner
- Control
- Floppy and Hard Disk Driver
- Disk Directory Searcher
- File Loader
- Error Handler and Displayer
- RS-232 Boot
- Diagnostic Package

Theory of Operation

This section describes the operation of various routines in the ROM Normally, the ROM is not addressable by normal use However, there are several routines that are available through fixed calling locations and these may be used by operating systems that are booting

On a power-up or RESET condition, the Z80 s program counter is set to address 0 and the boot ROM is switched-in The memory map of the system is set to Mode 0 (See Memory Map for details) This will cause the Z80 to fetch instructions from the boot ROM

The Initialization section of the Boot ROM now performs these functions:

1. Disables maskable and non-maskable interrupts
2. Interrupt mode 1 is selected
3. Programs the CRT Controller
4. Initializes the boot ROM control areas in RAM
5. Sets up a stack pointer
6. Issues a Force Interrupt to the Floppy Disk Controller to abort any current activity
7. Sets the system clock to 4mhz
8. Sets the screen to 64 x 16
9. Disables reverse video and the alternate character sets
10. Tests for · key being pressed*
11. Clears all 2K of video memory

* This is a special test If the · is being pressed then control is transferred to the diagnostic package in the ROM All other keys are scanned via the Keyboard Scanner

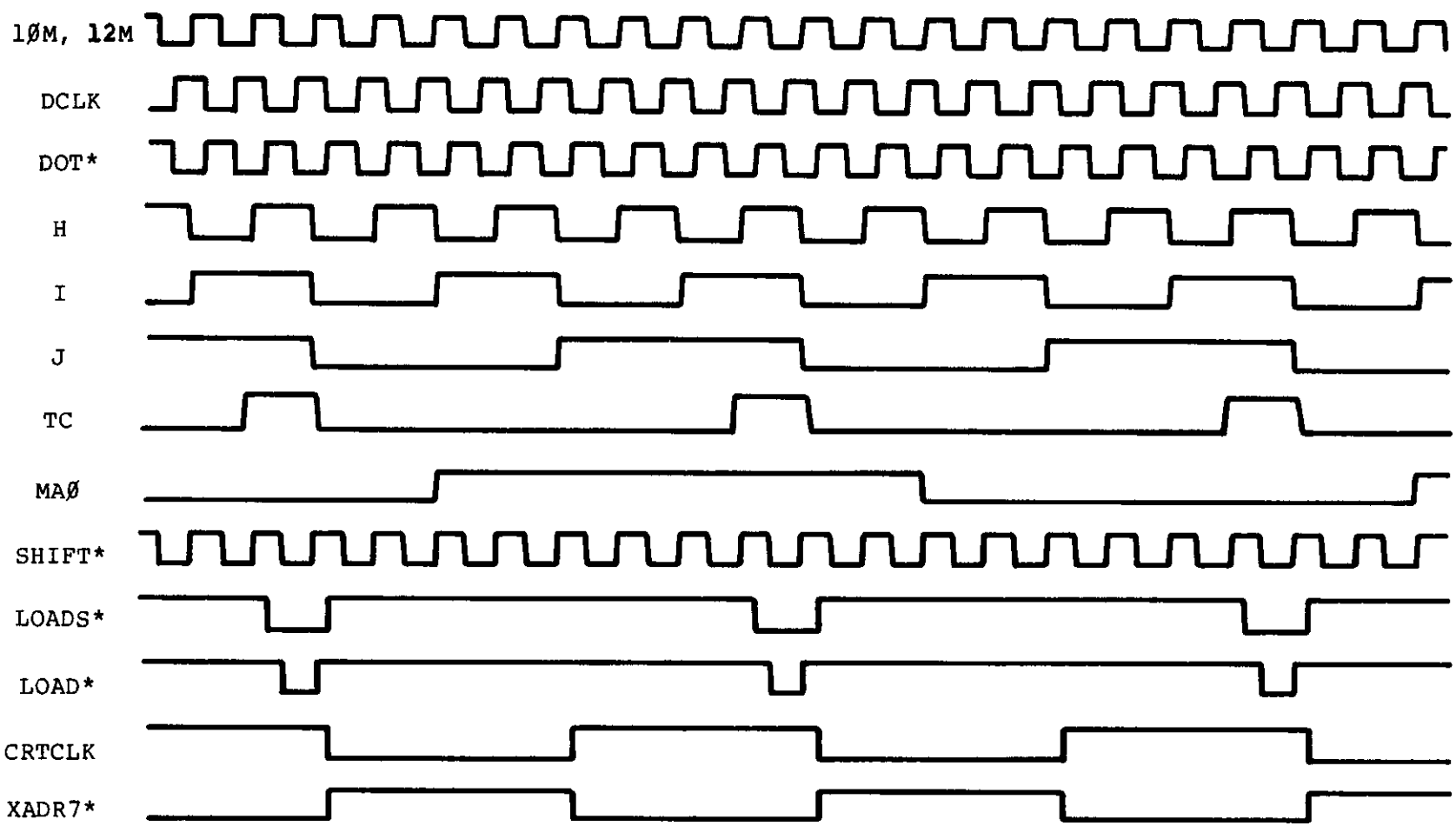


Figure 3-3. Video Timing 64 x 16 Mode 80 x 24 Mode

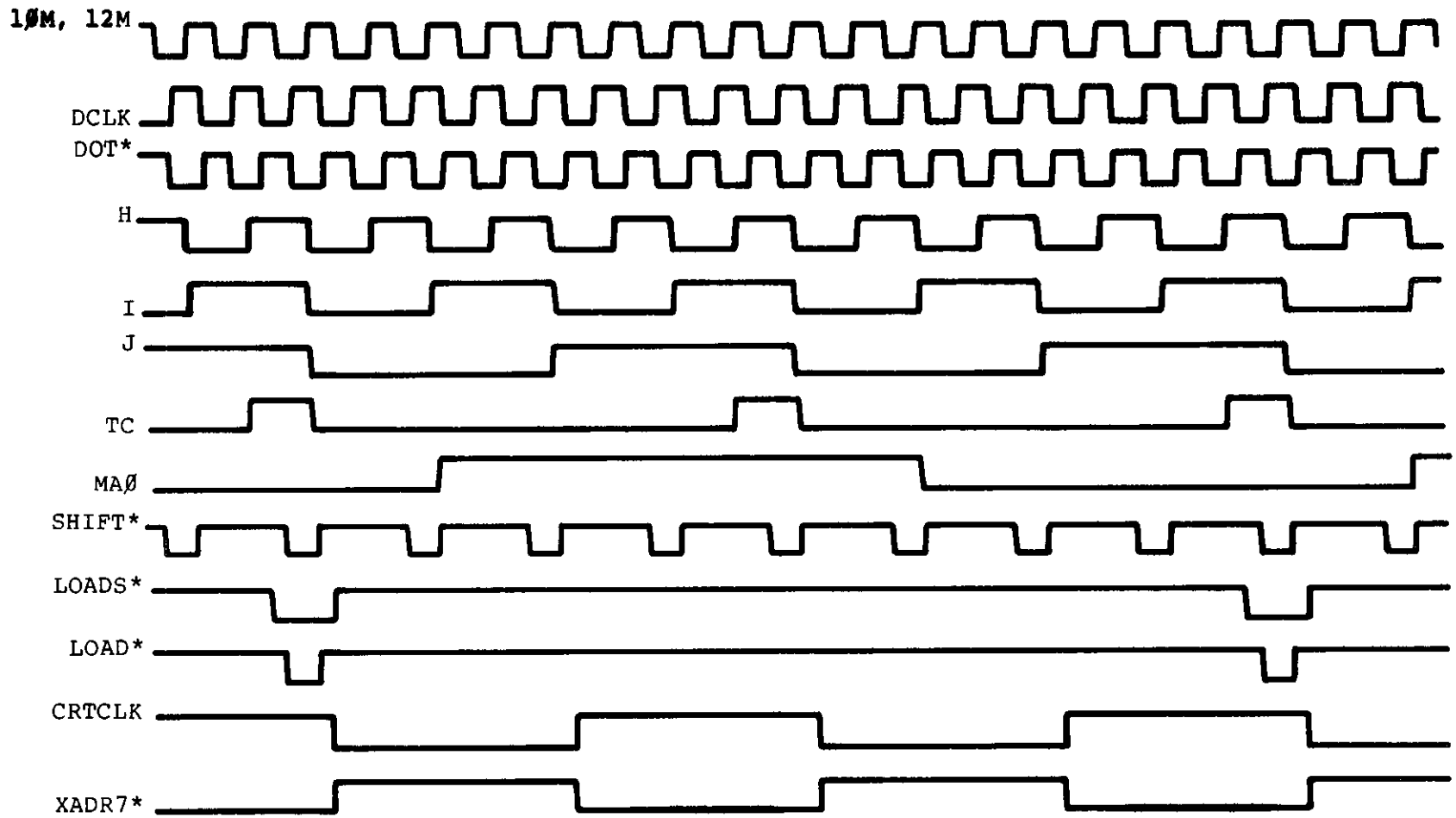


Figure 3-4. Video Timing 32 x 16 Mode 40 x 24 Mode

The Keyboard scanner is now called It scans the keyboard for a set period of time and returns several parameters based on which if any keys were pressed

The keyboard scanner checks for several different groups of keys These are shown below

Function Group	Selection Group
F1	A
<F2>	B
<F3>	C
<1>	D
<2>	E
<3>	F
<Left-Shift>	G
<Right-Shift>	
<Ctrl>	
<Caps>	

Special Keys	Misc Keys
<P>	Enter
<L>	Break
<N>	

When any key in the Function Group is pressed it is recorded in RAM and will be used by the Control routine in directing the action of the boot If more than one of these keys are pressed during the keyboard scan the last one detected will be the one that is used The Function group keys are currently defined as

<F1> or <1>	Will cause hard disk boot
<F2> or <2>	Will cause floppy disk boot
<F3> or <3>	Will force Model III mode
<Left-Shift>	Reserved for future use
<Right-Shift>	Boot from RS-232 port
<Ctrl>	Reserved for future use
<Caps>	Reserved for future use

The Special keys are commands to the Control routine which direct handling of the Model III ROM-image Each key is detected individually

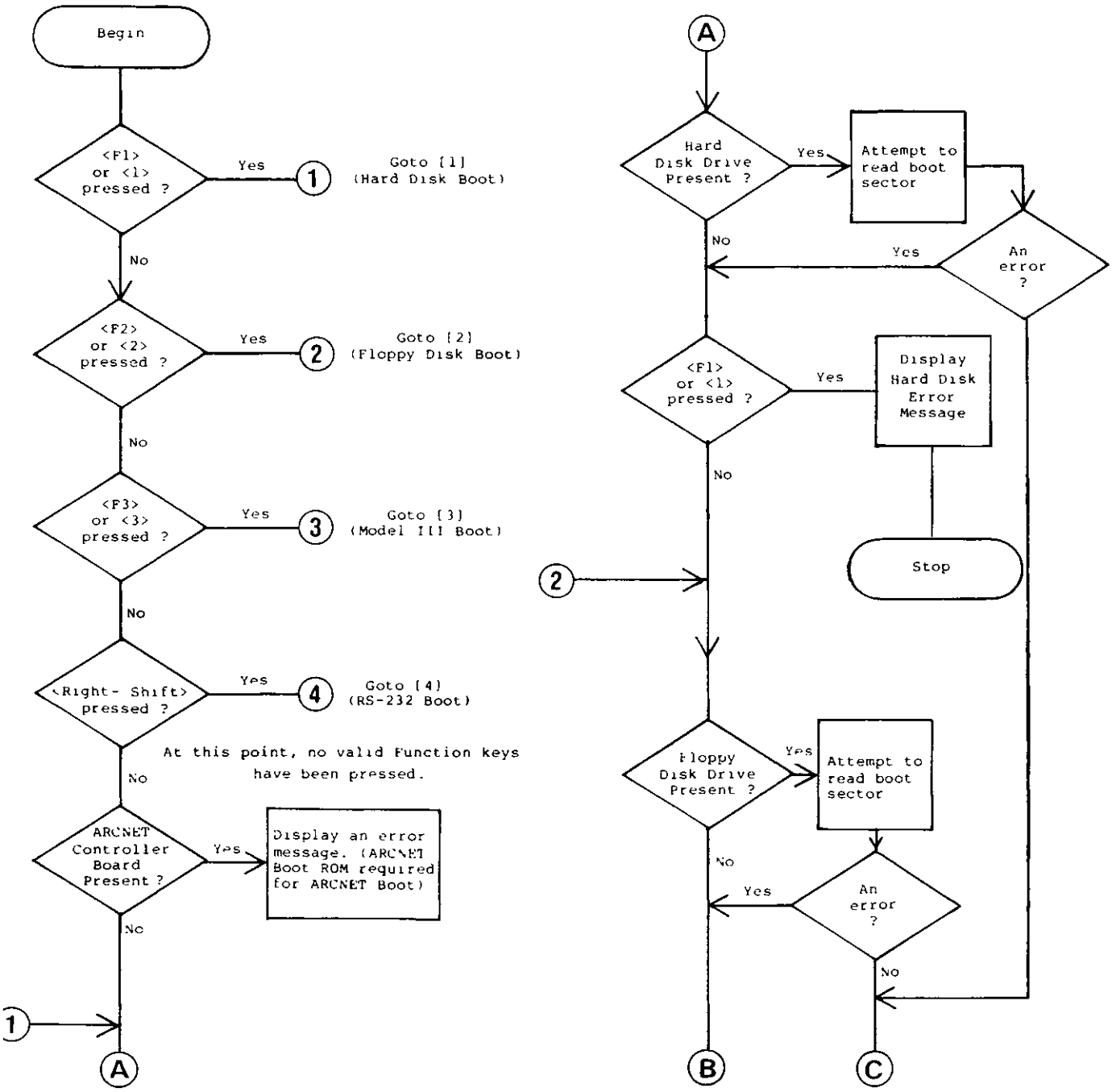
<P>	When loading the Model III ROM image the user will be prompted when the disks can be switched or when ROM BASIC can be entered by pressing Break
<N>	Instructs the Control routine to not load the Model III ROM image even if it appears that the operating system being booted requires it
L	Instructs the Control routine to load the Model III ROM image even if it is already loaded This is useful if the ROM image has been corrupted or when switching ROM images (Note that this will not cause the ROM image to be loaded if the boot sector check indicates that the Model III ROM image is not needed Press F3 or F3 and L to accomplish that

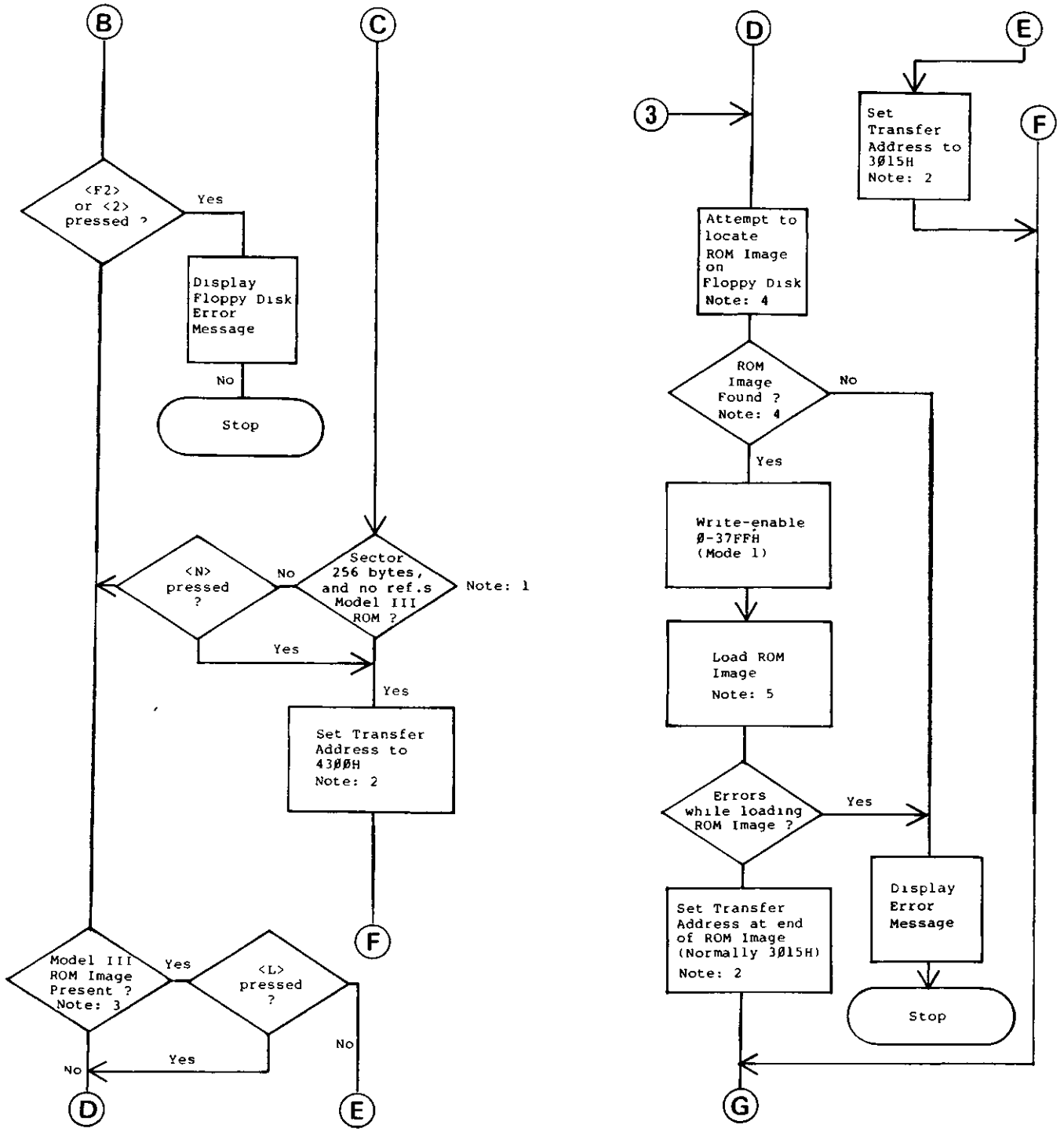
The Selection group keys are used in determining which file will be read from disk when the ROM image is loaded For details of this operation see the Disk Directory Searcher If more than one of the Selection group keys are pressed the last one detected will be the one that is used

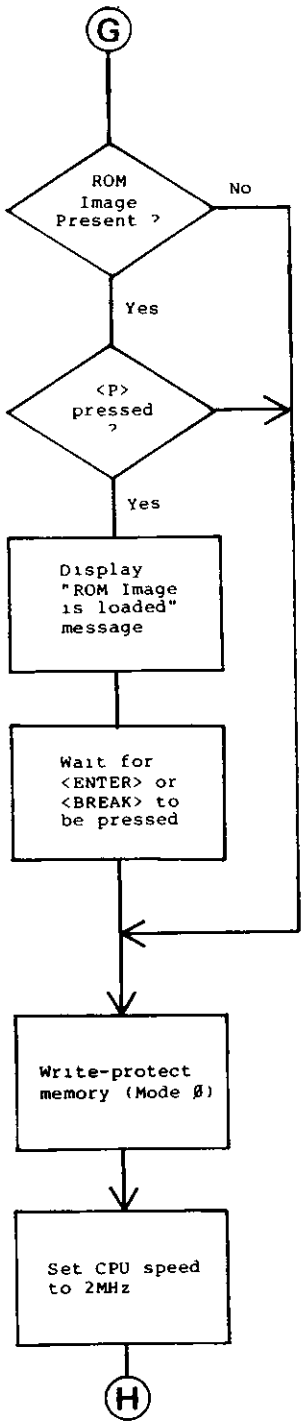
The Miscellaneous keys are

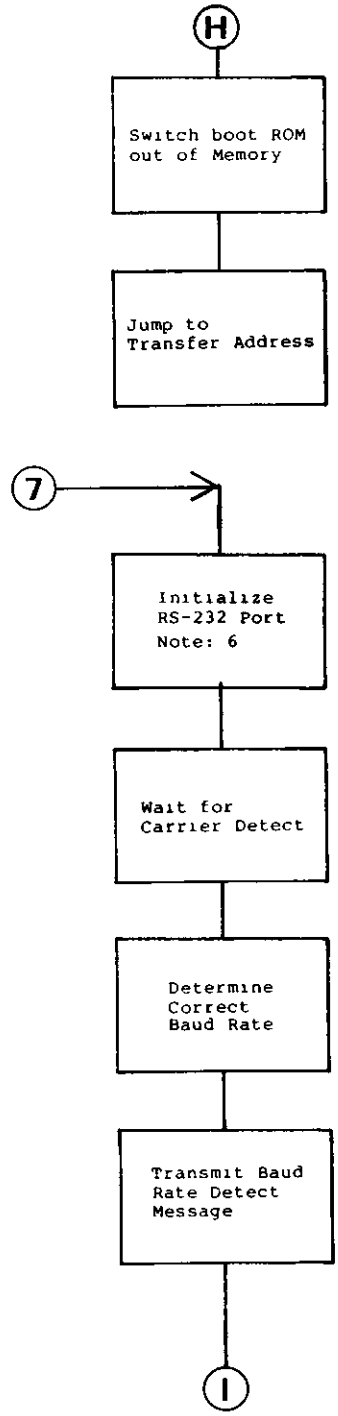
Break	Pressing this key is simply recorded by setting location 405BH non-zero It is up to an operating system to use this flag if desired
Enter	Terminates the Keyboard routine Any other keys pressed up to that time will be acted upon Enter is useful for experienced users who do not want to wait until the keyboard timer expires

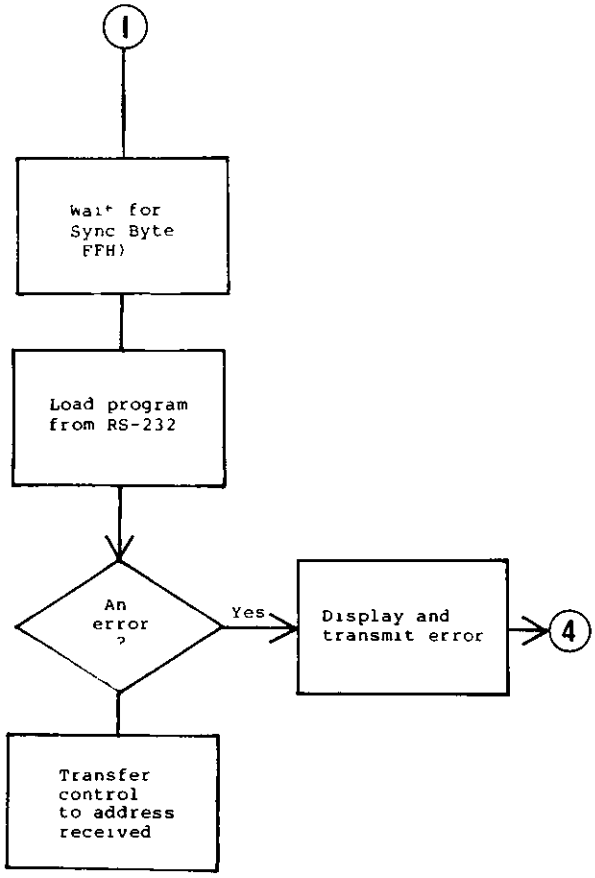
The Control section now takes over and follows the following flowchart


Begin
<F1> or <1> pressed ?
Yes
1
Goto [1] (Hard Disk Boot)
No
<F2> or <2> pressed ?
Yes
2
Goto [2] (Floppy Disk Boot)
No
<F3> or <3> pressed ?
Yes
3
Goto [3] (Model III Boot)
No
<Right- Shift> pressed ?
Yes
4
Goto [4] (RS-232 Boot)
At this point, no valid Function keys have been pressed.
No
ARCNET Controller Board Present ?
Yes
Display an error message. (ARCNET Boot ROM required for ARCNET Boot)
No
1
A
A
Hard Disk Drive Present ?
Yes
Attempt to read boot sector
No
Yes
An error ?
<F1> or <1> pressed ?
Yes
Display Hard Disk Error Message
Stop
No
2
Floppy Disk Drive Present ?
Yes
Attempt to read boot sector
No
Yes
An error ?
No
B
C


B
C
D
E
F
G
3
<F2> or <2> pressed ?
Yes
No
Display Floppy Disk Error Message
Stop
<N> pressed ?
No
Sector 256 bytes, and no ref.s Model III ROM ?
Note: 1
Yes
Yes
Set Transfer Address to 43ØØH
Note: 2
Model III ROM Image Present ? Note: 3
Yes
<L> pressed ?
No
Yes
No
Set Transfer Address to 3Ø15H
Note: 2
Attempt to locate ROM Image on Floppy Disk
Note: 4
ROM Image Found ? Note: 4
No
Yes
Write-enable Ø-37FFH (Mode 1)
Load ROM Image
Note: 5
Errors while loading ROM Image ?
Yes
Set Transfer Address at end of ROM Image (Normally 3Ø15H)
Note: 2
Display Error Message
Stop


G
ROM Image Present ?
No
Yes
<P> pressed ?
Yes
Display "ROM Image is loaded" message
Wait for <ENTER> or <BREAK> to be pressed
Write-protect memory (Mode Ø)
Set CPU speed to 2MHz
H


H
Switch boot ROM out of Memory
Jump to Transfer Address
7
Initialize RS-232 Port Note: 6
Wait for Carrier Detect
Determine Correct Baud Rate
Transmit Baud Rate Detect Message
I



Notes

(1) If the boot sector was not 256 bytes in length then it is assumed to be a Model III package and the ROM image will be needed If the sector is 256 bytes in length then the sector is scanned for the sequence CDxx00H The CD is the first byte of a Z80 unconditional subroutine call The next byte can have any value The third byte is tested against a zero What this check does is test for any references to the first 256 bytes of memory All Radio Shack Model III operating systems and many other packages all reference the ROM at some point during the boot sector Most boot sectors will display a message if the system cannot be loaded To save space these routines use the Model III ROM calls to display the message Several ROM calls have their entry points in the first 256 bytes of memory and these references are detected by the boot ROM Packages that do not reference the Model III ROM in the boot sector can still cause the Model III ROM image to be loaded by coding a CDxx00 somewhere in the boot sector It does not have to be executable At the same time Model 4 packages must take care that there is no sequence of bytes in the boot sector that could be mis interpreted to be a reference to the Boot ROM An example of this would be sequence 06CD0E00 which is a LD B 0CDH and a LD C 0 If the boot sector cannot be changed then the user must press the F3 key each time the system is started to inform the ROM that the d sk contains a Model III package which needs the Model III ROM image

(2) If you are loading a Model 4 operating system then the boot ROM will always transfer control to the first byte of the boot sector which is at 4300H If you are loading a Model III operating system or about to use Model III ROM BASIC then the transfer address is 3015H This is the address of a jump vector in the C ROM of the Model III ROM image and this will cause the system to behave exactly like a Model III If the ROM image file that is loaded has a different transfer address then that address will be used when loading is complete If the image is already present the Boot ROM will use 3015H

(3) Two different tests are done to insure that the Model III ROM image is present The first test is to check every third location starting at 3000H for a C3H This is done for 10 locations If any of these locations does not contain a C3H then the ROM image is considered to be not present The next test is to check two bytes at location 000BH If these addresses contain E9E1H then the ROM image is considered to be present

(4) See Disk Director Searcher for more information

(5) See File Loader for more information

(6) The RS 232 loader is described under RS 232 Boot

Disk Directory Searcher

When the Model III ROM image is to be loaded it is always read from the floppy in drive 0

Before the operation begins some checks are made First the boot sector is read in from the floppy and the first byte is checked to make sure it is either a 00H or a FEH If the byte contains some other value no attempt will be made to read the ROM image from that disk The location of the directory cylinder is then taken from the boot sector and the type of disk is determined This is done by examining the Data Address Mark that

was picked up by the Floppy Disk Controller (FDC) during the read of the sector If the DAM equals 1 the disk is a TRSDOS 1 x style disk If the DAM equals 0 then the disk is a LDOS 5 1 TRSDOS 6 style disk This is important since TRSDOS 1 x disks number sectors starting with 1 and LDOS style disks number sectors starting with 0

Once the disk type has been determined an extra test is made if the disk is a LDOS style disk This test reads the Granule Allocation Table (GAT) to determine if the disk is single sided or double sided

The directory is then read one record at a time and a compare is made against the pattern 'MODEL% for the filename and 'III' for the extension The '% means that any character will match this position If the user pressed one of the selection keys (A-G) during the keyboard scan, then that character is substituted in place of the '% character For example, if you pressed 'D', then the search would be for the file MODELD , with the extension 'III' The searching algorithm searches until it finds the entry or it reaches the end of the directory

Once the entry has been found, the extent information for that file is copied into a control block for later use

File Loader

The file loader is actually two modules — the actual loader and a set of routines to fetch bytes from the file on disk The loader is invoked via a RST 28H The byte fetcher is called by the loader using RST 20H Since restart vectors can be re-directed, the same loader is used by the RS-232 boot The difference is that the RST 20H is redirected to point to the RS-232 data receiving routine The loader reads standard loader records and acts upon two types

01 Data Load
1 byte with length of block, including address
1 word with address to load the data
n bytes of data, where n + 2 equals the length specified

02 Transfer Address
1 byte with the value of 02
1 word with the address to start execution at

Any other loader code is treated as a comment block and is ignored Once an 02 record has been found, the loader stops reading, even if there is additional data, so be sure to place the 02 record at the end of the file

Floppy and Hard Disk Driver

The disk drivers are entered via RST 8H and will read a sector anywhere on a floppy disk and anywhere on head 1 (top-head) in a hard disk drive Either 256 or 512 byte sectors are readable by these routines and they make the determination of the sector size The hard disk driver is compatible with both the WD1000 and the WD1010 controllers The floppy disk driver is written for the WD1793 controller

Serial Loader

Invoking the serial loader is similar to forcing a boot from hard disk or floppy In this case the right shift key must be pressed at some time during the first three seconds after reset The program does not care if the key is pressed forever making it convenient to connect pins 8 and 10 of the keyboard connector with a shorting plug for bench testing of boards This assumes that the object program being loaded does not care about the key closure

Upon entry, the program first asserts DTR (J4 pin 20) and RTS (J4 pin 4) true Next, Not Ready is printed on the topmost line of the video display Modem status line CD (J4 pin 8) is then sampled The program loops until it finds CD asserted true At that time the message "Ready" is displayed Then the program sets about determining the baud rate from the host computer

To determine the baud rate, the program compares data received by the UART to a test byte equal to 55 hex The receiver is first set to 19200 baud If ten bytes are received which are not equal to the test byte the baud rate is reduced This sequence is repeated until a valid test byte is received If ten failures occur at 50 baud, the entire process begins again at 19200 baud If a valid test byte is received, the program waits for ten more to arrive before concluding that it has determined the correct baud rate If at this time an improper byte is received or a receiver error (overrun, framing, or parity) is intercepted, the task begins again at 19200 baud

In order to get to this point the host or the modem must assert CD true The host must transmit a sequence of test bytes equal to 55 hex with 8 data bits odd parity and 1 or 2 stop bits The test bytes should be separated by approximately 0 1 second to avoid overrun errors

When the program has determined the baud rate, the message

"Found Baud Rate x"

is displayed on the screen where ' x" is a letter from A to P meaning

A = 50 baud	E = 150	I = 1800	M = 4800
B = 75	F = 300	J = 2000	N = 7200
C = 110	G = 600	K = 2400	O = 9600
D = 134 5	H = 1200	L = 3600	P = 19200

The same message less the character signifying the baud rate is transmitted to the host, with the same baud rate and protocol This message is the signal to the host to stop transmitting test bytes

After the program has transmitted the baud rate message it reads from the UART data register in order to clear any overrun error that may have occurred due to the test bytes coming in during the transmission of the message This is because the receiver must be made ready to receive a sync byte signalling the beginning of the command file For this reason it is important that the host wait until the entire baud rate message (16 characters) is received before transmitting the sync byte which is equal to FF hex

When the loader receives the sync byte the message

"Loading'

is displayed on the screen Again, the same message is transmitted to the host, and, again the host must wait for the entire transmission before starting into the command file

If the receiver should intercept a receive error while waiting for the sync byte, the entire operation up to this point is aborted The video display is cleared and the message

"Error, x'

is displayed near the bottom of the screen, where x is a letter from B to H, meaning

B = parity error
C = framing error
D = parity & framing errors
E = overrun error
F = parity & overrun errors
G = framing & overrun errors
H = parity & framing & overrun errors

The message

"Error"

is then transmitted to the host The entire process is then repeated from the ' Not Ready' message A six second delay is inserted before reinitialization This is longer than the time required to transmit five bytes at 50 baud, so there is no need to be extra careful here

If the sync byte is received without error, then the "Loading' message is transmitted and the program is ready to receive the command file After receiving the ' Loading message the host can transmit the file without nulls or delays between bytes

(Since the file represents Z80 machine code and all 256 combinations are meaningful it would be disastrous to transmit nulls or other ASCII control codes as fillers acknowledgement or start-stop bytes The only control codes needed are the standard command file control bytes)

Data can be transmitted to the loader at 19200 baud with no delays inserted Two stop bits are recommended at high baud rates

See the File Loader description for more information on file loading

If a receive error should occur during file loading the abort procedure described above will take place, so when attempting remote control, it is wise to monitor the host receiver during transmission of the file When the host is near the object board as is the case in the factory application or when more than one board is being loaded, it may be advantageous or even necessary to ignore the transmitted responses of the object board(s) and to manually pace the test byte, sync byte and command file phases of the transmission process using the video display for handshaking

System Programmers Information

The Model 4P Boot ROM uses two areas of RAM while it is running These are 4000H to 40FFH and 4300H to 43FFH (For 512 byte boot sectors, the second area is 4300H to 44FFH) If the Model III ROM Image is loaded additional areas are used See the technical reference manual for the system you are using for a list of these areas

Operating systems that want to support a software restart by re-executing the contents of the boot ROM can accomplish this in one of two ways If the operating system relies on the Model III ROM Image, then jump to location 0 as you have in the past If the operating system is a Model 4 mode package, a simple way is to code the following instructions in your assembly and load them before you want to reset

Absolute Location	Instruction	
0000	DI	
0001	LD	A 1
0003	OUT	(9CH) A

These instructions cause the boot ROM to become addressable After executing the OUT instruction the next instruction executed will be one in the boot ROM (These instructions also exist in the Model III ROM image at location 0) The boot ROM has been written so that the first instruction is at address 0005 The hardware must be in memory mode 0 or 1, or else the boot ROM will not be switched in This operation can be done with an OUT instruction and then a RST 0 can be executed to have the ROM switched in

Restarts can be redirected at any time while the ROM is switched in All restarts jump to fixed locations in RAM and these areas may be changed to point to the routine that is to be executed

Restart	RAM Location	Default Use
0	none	Cold Start Boot
8	4000H	Disk I O Request
10	4003H	Display string
18	4006H	Display block
20	4009H	Byte Fetch (Called by Loader)
28	400CH	File Loader
30	400FH	Keyboard scanner
38	4012H	Reserved for future use
66	4015H	NMI (Floppy I O Command Complete)

The above routines have fixed entry parameters These are described here

Disk I/O Request (RST 8H)

Accepts

A	1 for floppy 2 for hard disk	
B	Command	
	Initialize	1
	Restore	4
	Seek	6
	Read	12 (All reads have an implied seek)
C	Sector number to read The contents of the location disktype (405CH) are added to this value before an actual read If the disk is a two sided floppy just add 18 to the sector number	
DE	Cylinder number (Only E is used in floppy operations)	
HL	Address where data from a read operation is to be stored	

Returns

Z	Success Operation Completed
NZ	Error Error code in A

Error Codes

3	Hard Disk drive is not ready
4	Floppy disk drive is not ready
5	Hard Disk drive is not available
6	Floppy disk drive is not available
7	Drive Not Ready and no Index (Disk in drive door open)
8	CRC Error
9	Seek Error
11	Lost Data
12	ID Not Found

Display String (RST 10H)

Accepts

HL	Pointer to text to be displayed Text must be terminated with a null (0)
DE	Offset position on screen where text is to be displayed (A 0000H will be the upper left-hand corner of the display)

Returns
Success Always

A	Altered
DE	Points to next position on video
HL	Points to the null (0)

Display Block (RST 18H)

Accepts

HL	Points to control vector in the format		
	+0	Screen Offset	
	+2	Pointer to text, terminated with null	
	+4	Pointer to text terminated with null	
	+n	word FFFFH	End of control vector
or	+n	word FFFEH	Next word is new Screen Offset

If Z flag is set on entry, then the first screen offset is read from DE instead of from the control vector

Each string is positioned after the previous string unless a FFFEH entry is found This is used heavily in the ROM to reduce duplication of words in error messages

Returns
Success Always

DE	Points to next position on video

Byte Fetch (RST 20H)

Accepts None
Returns

Z	Success byte in A
NZ	Failure error code in A

Errors

	Any errors from the disk I O call and
2	ROM Image can t be loaded — Too many extents
10	ROM Image can t be loaded — Disk drive is not ready

File Loader (RST 28H)

Accepts None

Returns

Z	Success
NZ	Failure, error code in A

Errors

	Any errors from the disk I/O call or the byte fetch call and:
0	The ROM image was not found on drive 0

There are several pieces of information left in memory by the boot ROM which are useful to system programmers. These are shown below:

RAM Location	Description
401DH	ROM Image Selected (% for none selected or A-G)
4055H	Boot type 1 = Floppy 2 = Hard disk 3 = ARCNET 4 = RS-232C 5 - 7 = Reserved
4056H	Boot Sector Size (1 for 256, 2 for 512)
4057H	RS-232 Baud Rate (only valid on RS-232 boot)
4059H	Function Key Selected 0 = No function key selected <F1> or <1> 86 <F2> or <2> 87 <F3> or <3> 88 <Caps> 85 <Ctrl> 84 <Left-Shift> 82 <Right-Shift> 83 Reserved 80-81 and 89-90
405BH	Break Key Indication (non-zero if <Break> pressed)
405CH	Disk type (0 for LDOS TRSDOS 6.1 for TRSDOS 1.x)

Keep in mind that Model III ROM image will initialize these areas, so this information is useful only to the Model 4 mode programmer.

3.1.7 RAM

Two configurations of Random Access Memory (RAM) are available on the Model 4P: 64K and 128K. The 64K and 128K option use the 6665-type 64K x 1 200NS Dynamic RAM, which requires only a single - 5v supply voltage.

The DRAMs require multiplexed incoming address lines. This is accomplished by ICs U111 and U112 which are 74LS157 multiplexers. Data to and from the DRAMs are buffered by a 74LS245 (U117) which is controlled by Page Map PAL, U110. The proper timing signals RAS0*, RAS1*, MUX*, and CAS* are generated by a delay line circuit U97. U115 (1 2 of a 74S112) and U116 (1 4 of a 74F08) are used the generate a precharge circuit. During M1 cycles of the Z80A in 4 MHz mode, the high time in MREQ has a minimum time of 110 nanosecs. The specification of 6665 DRAM requires a minimum of 120 nanosecs so this circuit will shorten the MREQ signal during the M1 cycle. The resulting signal PMREQ is used to start a RAM memory cycle through U113 (a 74S64). Each different cycle is controlled at U113 to maintain a fast M1 cycle so no wait states are required. The output of U113 (PRAS*) is ANDed with RFSH to not allow MUX* and CAS* to be generated during a REFRESH cycle. PRAS* also generates either RAS0* or RAS1*, depending on which bank of RAM the CPU is selecting. GCAS* generated by the delay line U97 is latched by U115 (1 2 of a 74S112) and held to the end of the memory cycle. The output of U115 is ANDed with VIDEO signal to disable the CAS* signal from occurring if the cycle is a video memory access. Refer to **M1 Cycle Timing (Figure 3-8. and 3-9.), Memory Read and Memory Write Cycle Timing (Figure 3-10.) and (Figure 3-11.).**

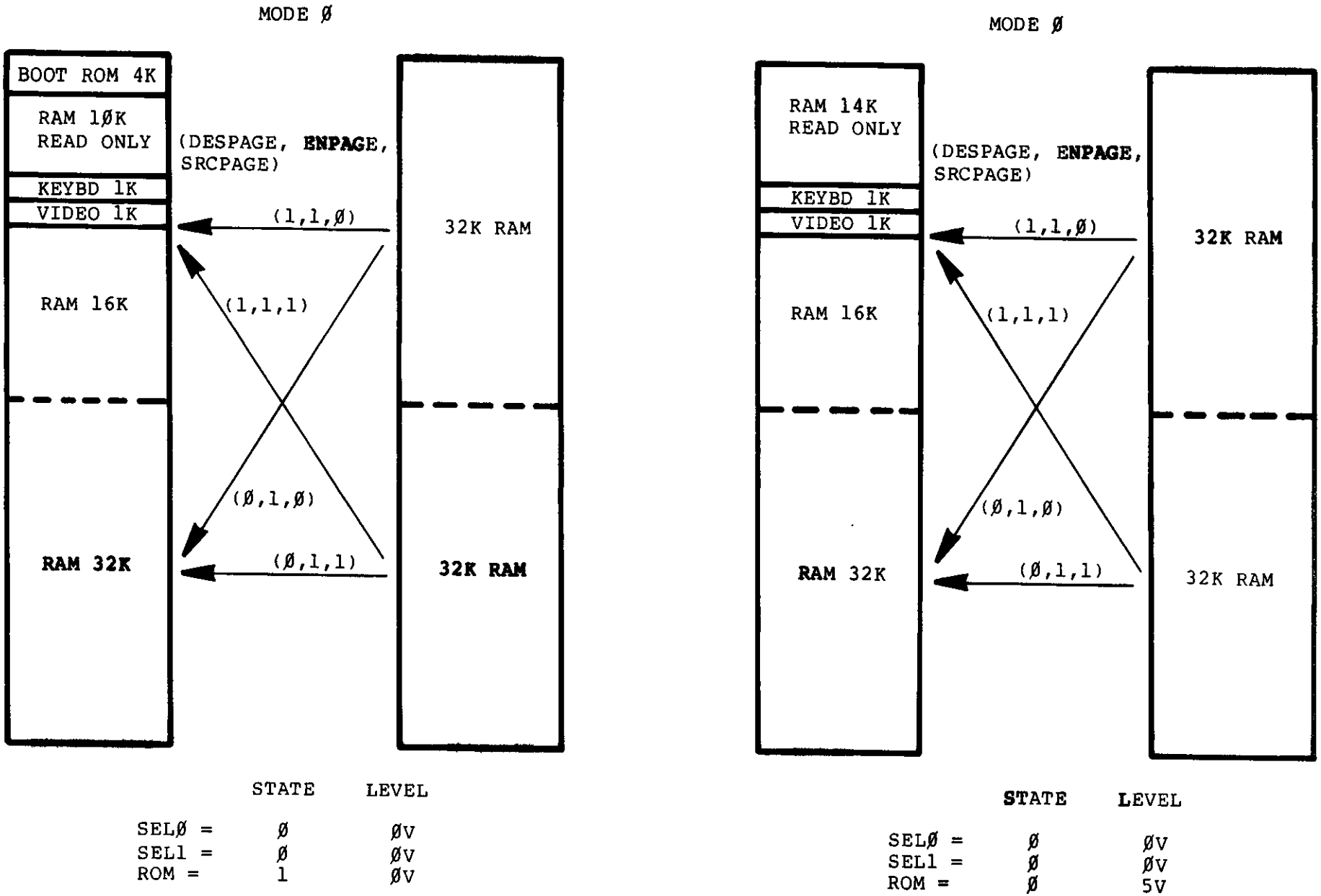


Figure 3-5. Memory

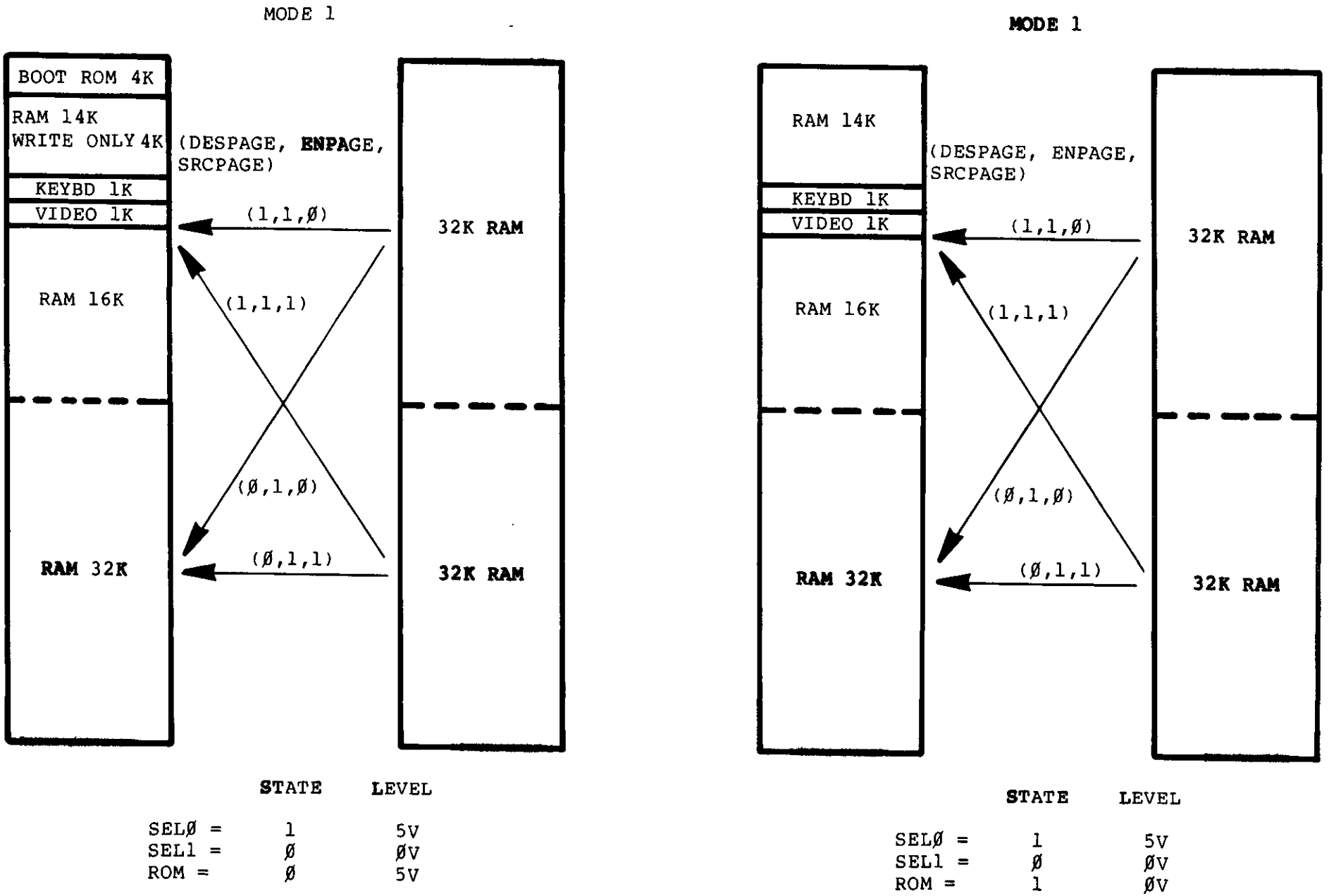
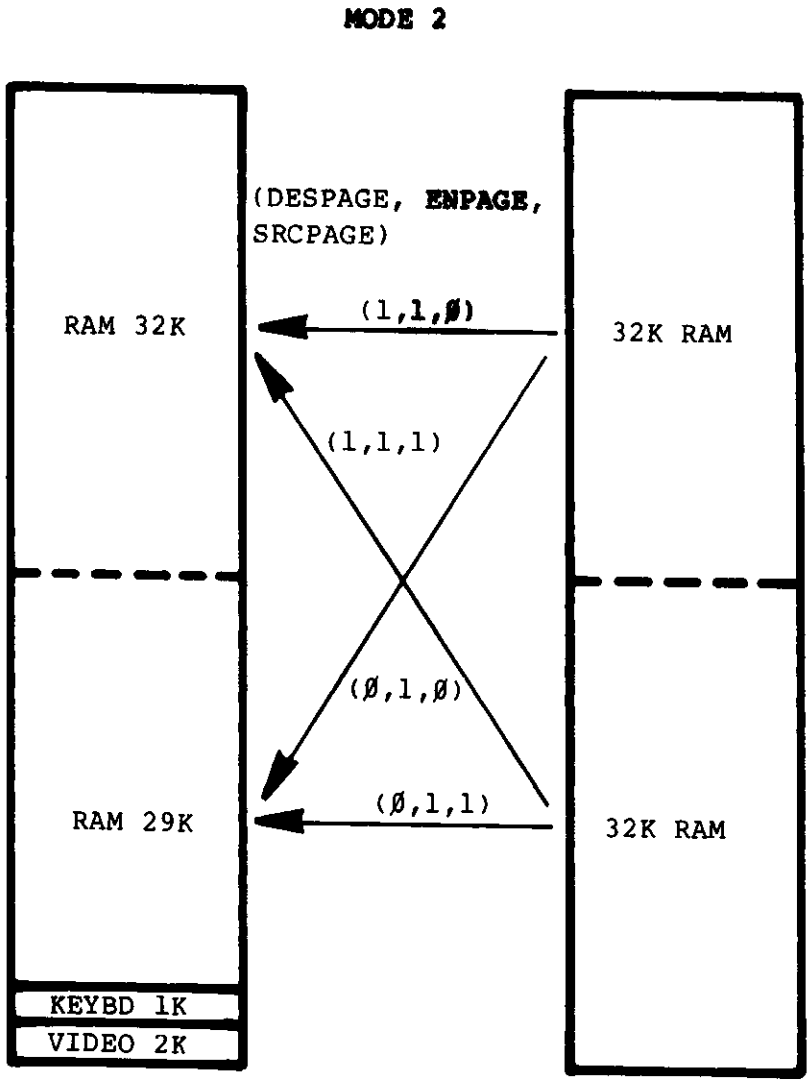


Figure 3-6. Memory



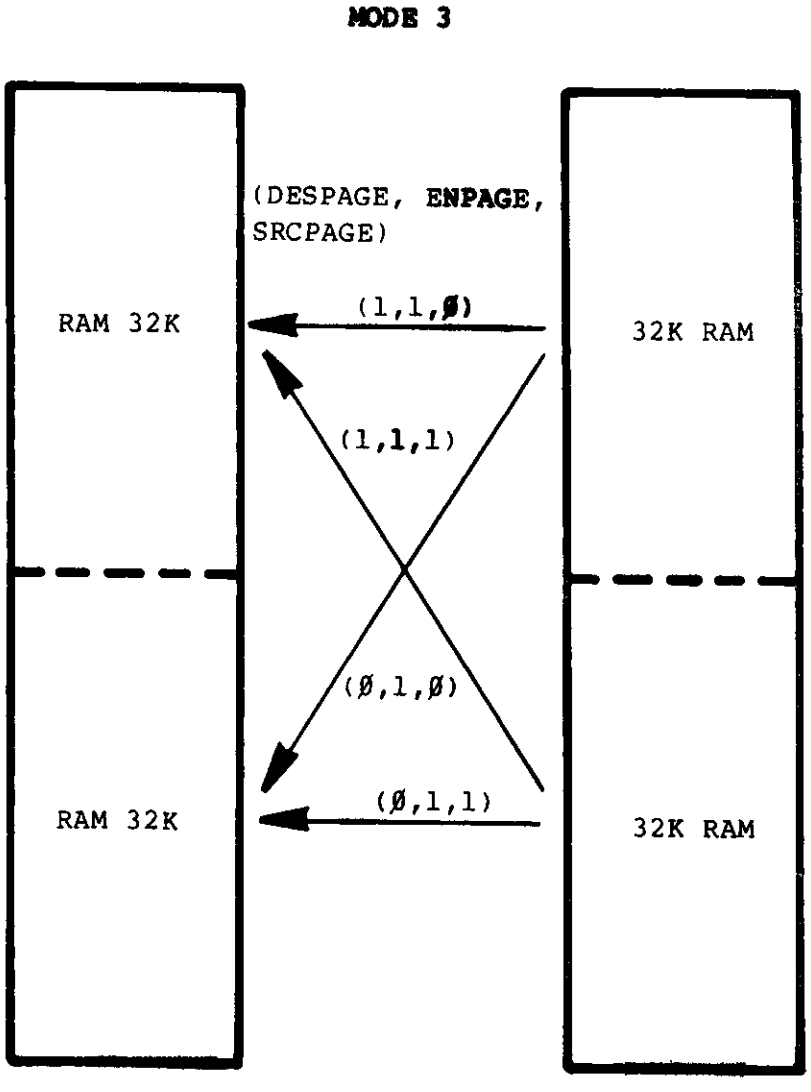


Figure 3-7. Memory

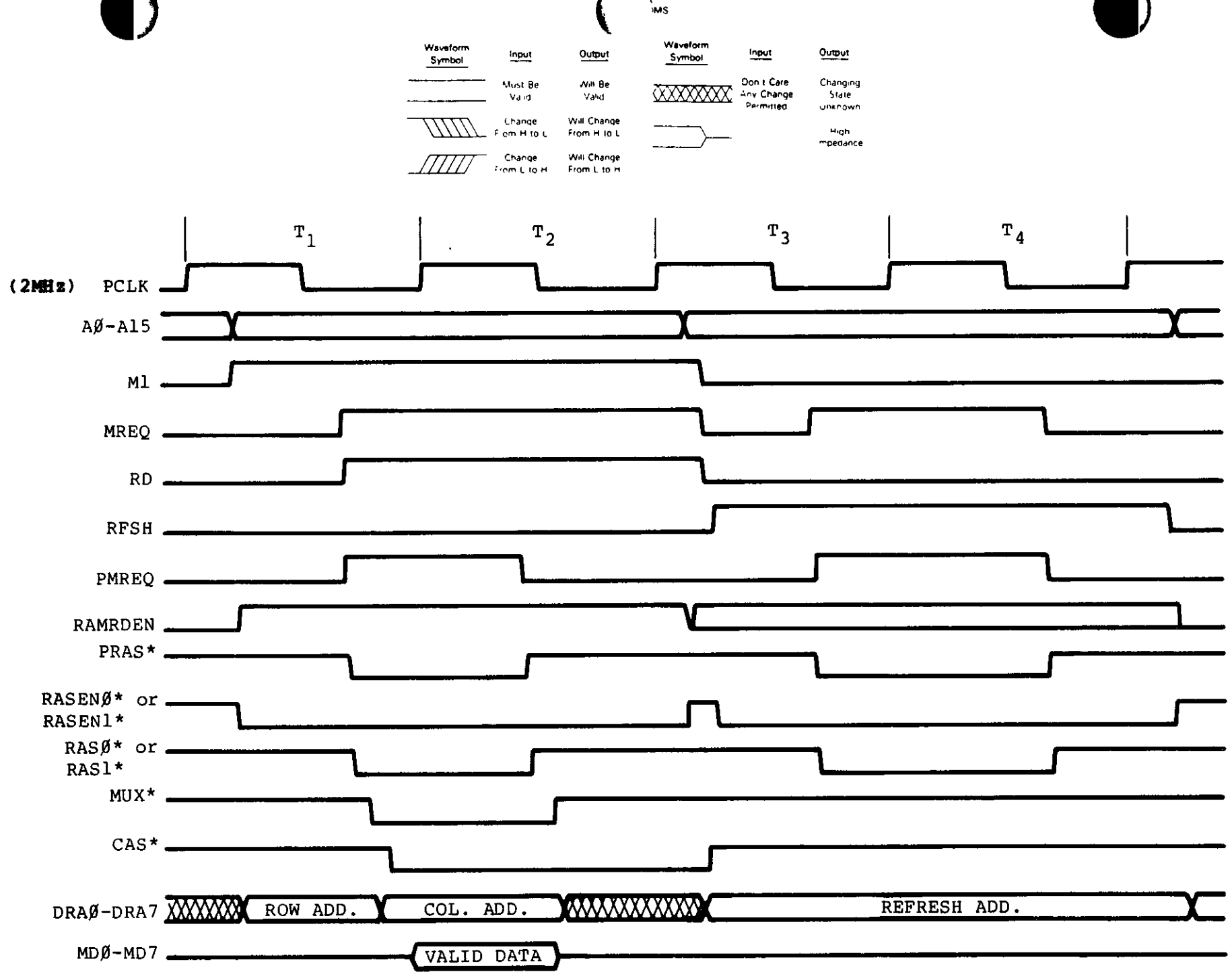


Figure 3-8. M1 Cycle Timing (2MHZ) 100ns/dir.

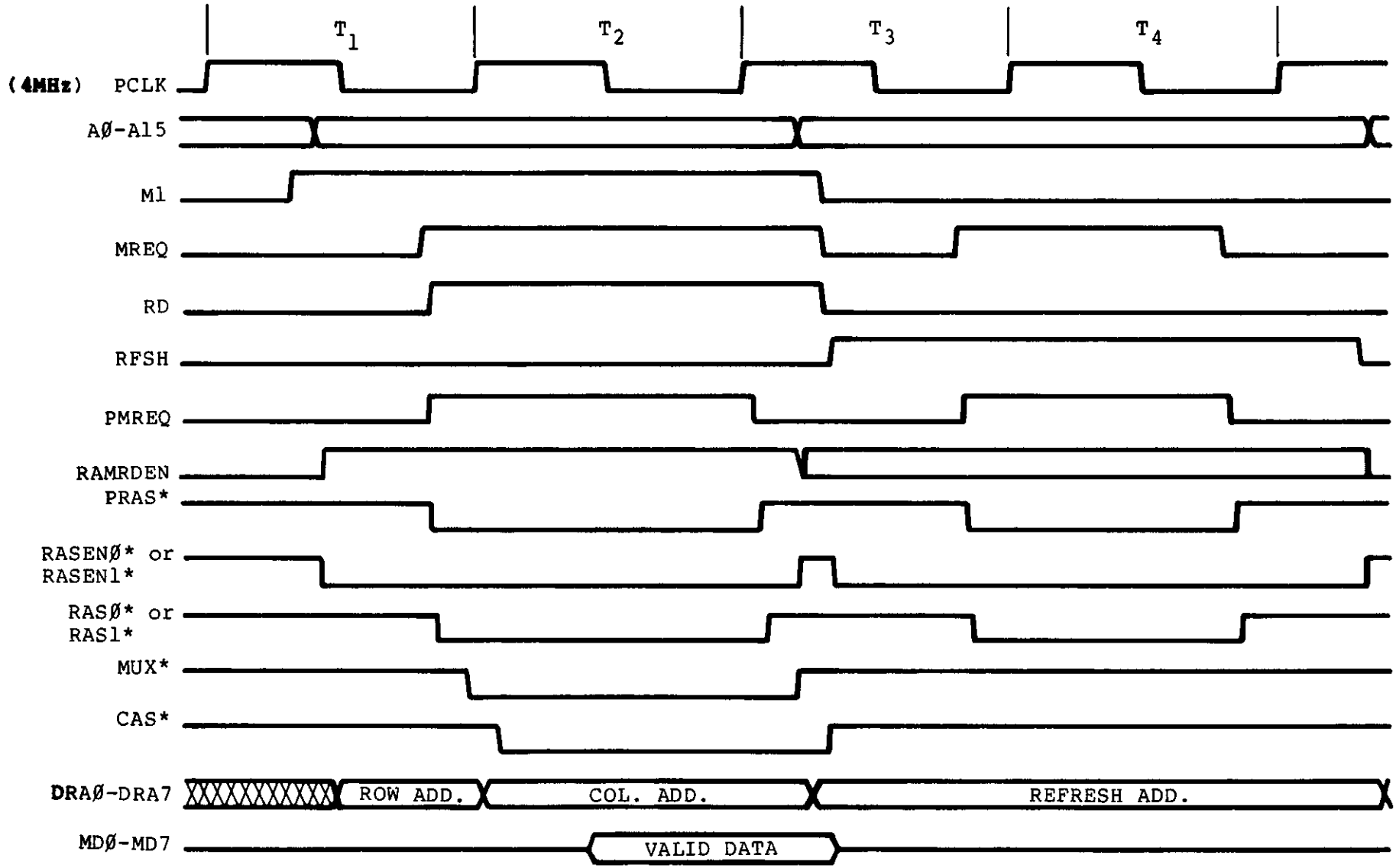


Figure 3-9. M1 Cycle Timing (4MHZ) 50ns/dir.

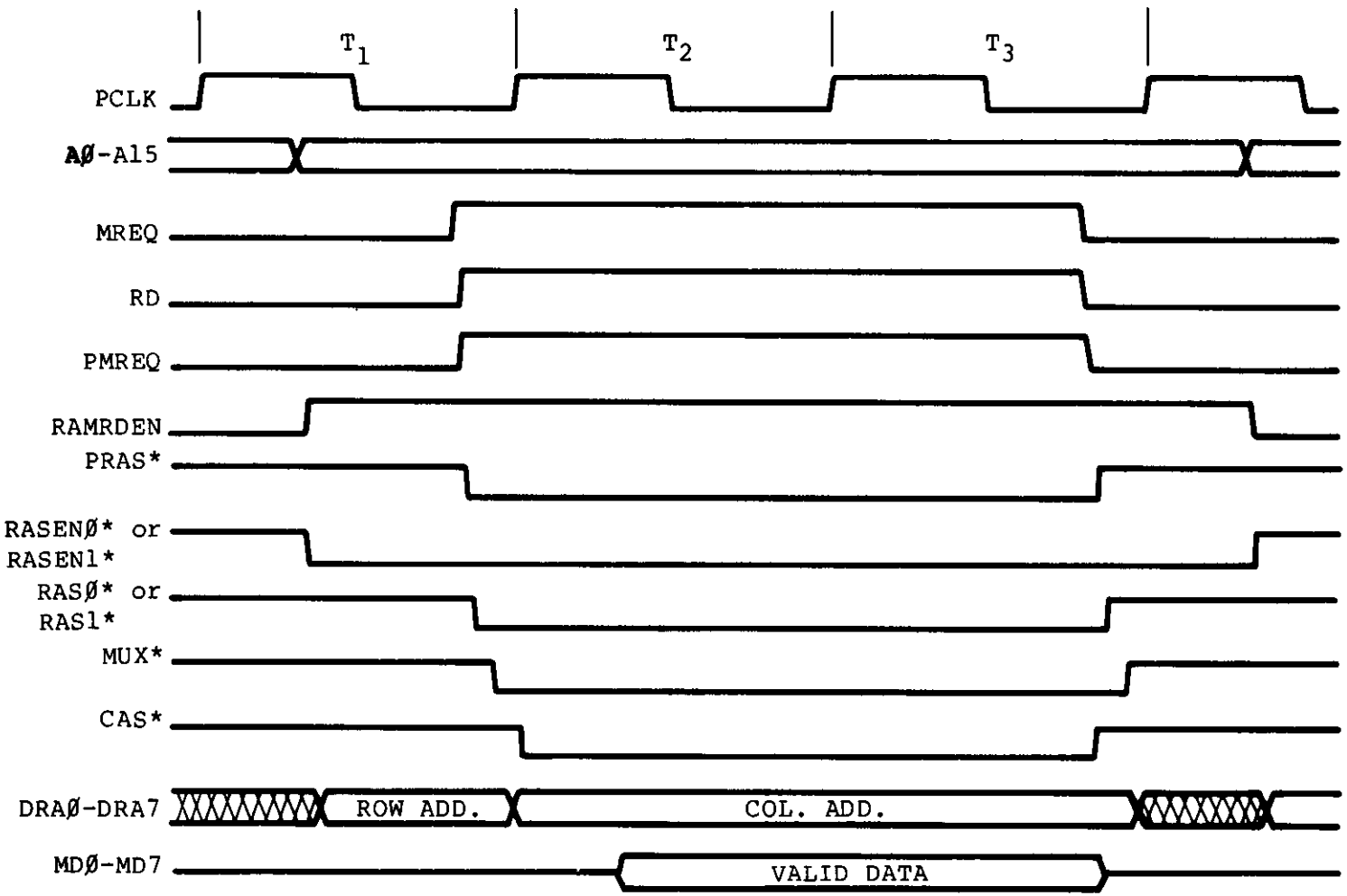


Figure 3-10. Memory Read Cycle Timing

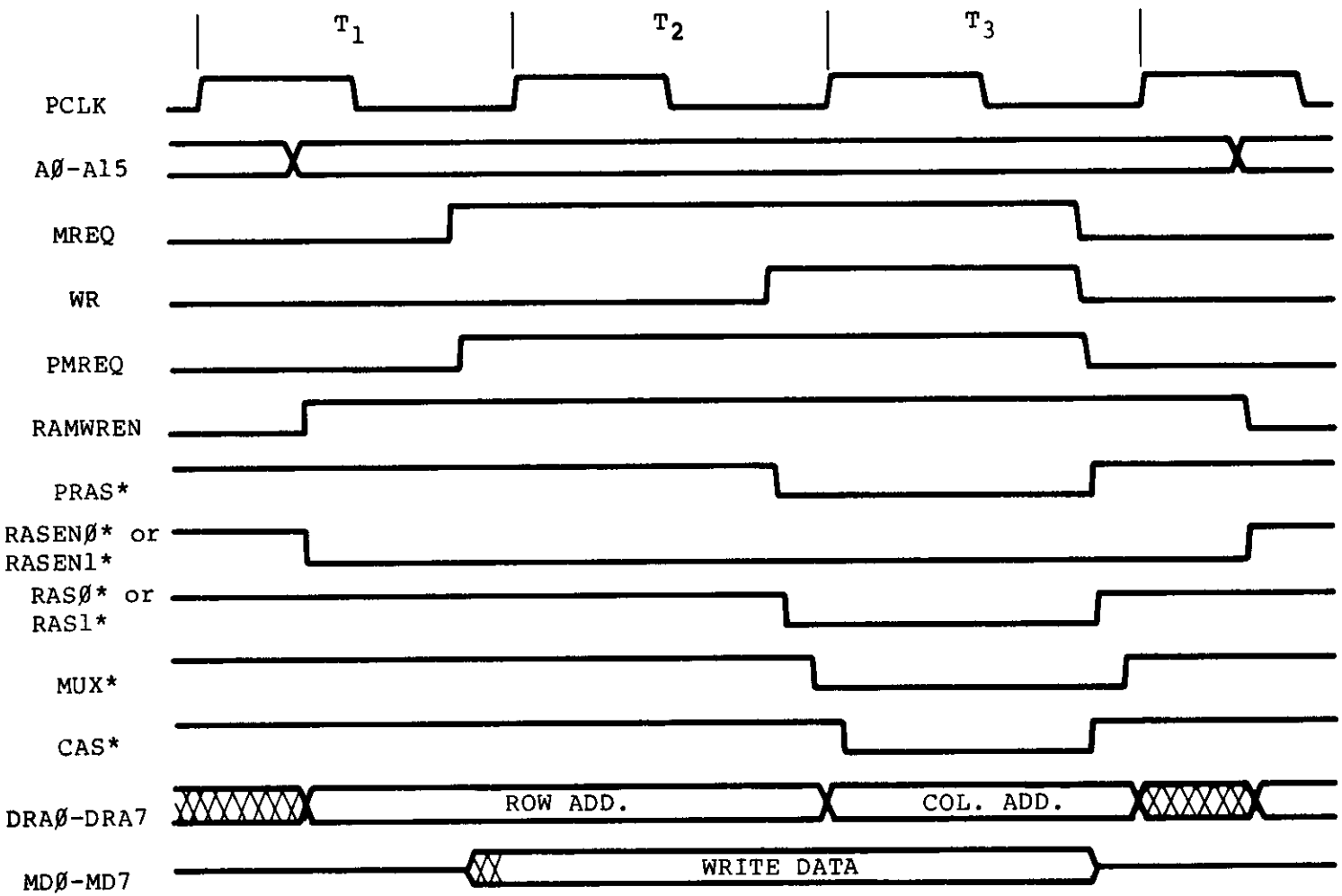


Figure 3-11. Memory Write Cycle Timing

Mode 0

SEL0	0	0V
SEL1	0	0V
ROM	1	0V

0000 — 0FFF	Boot ROM	4K
1000 — 37FF	RAM (Read Only)	10K
37E8 — 37E9	Printer Status (Read Only)	2
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 0

SEL0	0	0V
SEL1	0	0V
ROM	0	+5V

0000 — 37FF	RAM (Read Only)	14K
37E8 — 37E9	Printer Status (Read Only)	2
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 1

SEL0	1	+5V
SEL1	0	0V
ROM	1	0V

0000 — 0FFF	Boot ROM	4K
0000 — 0FFF	RAM (Write Only)	4K
1000 — 37FF	RAM	10K
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 1

SEL0	1	+5V
SEL1	0	0V
ROM	0	+5V

0000 — 37FF	RAM	**14K**
3800 — 3BFF	Keyboard	**1K**
3C00 — 3FFF	Video	**1K**
4000 — FFFF	RAM	**48K**

Mode 2

SEL0	0	0V
SEL1	1	+5V
ROM	X	Don't Care

0000 — F3FF	RAM	**61K**
F400 — F7FF	Keyboard	**1K**
F800 — FFFF	Video	**2K**

Mode 3

SEL0	1	+5V
SEL1	1	+5V
ROM	X	Don't Care

0000 — FFFF	RAM	**64K**

I/O Port Assignment

Port #	Normally Used	Out	In
FC — FF	FF	CASSOUT *	MODIN*
F8 — FB	F8	LPOUT *	LPIN*
F4 — F7	F4	DRVSEL *	(RESERVED)
F0 — F3	–	DISKOUT *	DISKIN *
F0	F0	FDC COMMAND REG.	FDC STATUS REG.
F1	F1	FDC TRACK REG.	FDC TRACK REG.
F2	F2	FDC SECTOR REG.	FDC SECTOR REG.
F3	F3	FDC DATA REG.	FDC DATA REG.
EC — EF	EC	MODOUT *	RTCIN *
E8 — EB	–	RS232OUT *	RS232IN *
E8	E8	UART MASTER RESET	MODEM STATUS
E9	E9	BAUD RATE GEN. REG.	(RESERVED)
EA	EA	UART CONTROL AND MODEM CONTROL REG.	UART STATUS REG.
EB	EB	UART TRANSMIT HOLDING REG.	UART HOLDING REG. (RESET D.R.)
E4 — E7	E4	WR NMI MASK REG. *	RD NMI STATUS *
E0 — E3	E0	WR INT MASK REG. *	RD INT MASK REG. *
A0 — DF	–	(RESERVED)	(RESERVED)
9C — 9F	9C	BOOT *	(RESERVED)
94 — 9B	–	(RESERVED)	(RESERVED)
90 — 93	90	SEN *	(RESERVED)
8C — 8F	–	GSEL0 *	GSEL0 *
88 — 8B	–	CRTCCS *	(RESERVED)
88, 8A	88	CRCT ADD. REG.	(RESERVED)
89, 8B	89	CRCT DATA REG.	(RESERVED)
84 — 87	84	OPREG *	(RESERVED)
80 — 83	–	GSEL1 *	GSEL1 *

I/O Port Description

Name: CASSOUT *
Port Address: FC — FF
Access: WRITE ONLY
Description: Output data to cassette or for sound generation

Note: The Model 4P **does not** support cassette storage. this port is only used to generate sound that was to be output via cassette port. The Model 4P sends data to onboard sound circuit.

D0 = Cassette output level (sound data output)

D1 = Reserved

D2 — D7 = Undefined

Name: MODIN * (CASSIN *)
Port Address: FC — FF
Access: READ ONLY
Description: Configuration Status

D0 = 0

D1 = CASSMOTORON STATUS

D2 = MODSEL STATUS

D3 = ENALTSET STATUS

D4 = ENEXTIO STATUS

D5 = (NOT USED)

D6 = FAST STATUS

D7 = 0

Name: LPOUT *
Port Address: F8 — FB
Access: WRITE ONLY
Description: Output data to line printer

D0 — D7 = ASCII BYTE TO BE PRINTED

Name: LPIN *
Port Address: F8 — FB
Access: READ ONLY
Description: Input line printer status

D0 — D3 – (RESERVED)

D4 = FAULT
1 = TRUE
0 = FALSE

D5 = UNIT SELECT
1 = TRUE
0 = FALSE

D6 = OUTPAPER
1 = TRUE
0 = FALSE

D7 = BUSY
1 = TRUE
0 = FALSE

Name: DRVSEL *
Port Address: F4 — F7
Access: WRITE ONLY
Description: Output FDC Configuration

Note: Output to this port will **ALWAYS** cause a 1-2 mscc. (Microsecond) wait to the Z80.

D0 = DRIVE SELECT 0

D1 = DRIVE SELECT 1

D2 = (RESERVED)

D3 = (RESERVED)

D4 = SDSEL
0 = SIDE 0
1 = SIDE 1

D5 = PRECOMPEN
0 = No write precompensation
1 = Write Precompensation enabled

D6 = WSGEN
0 = No wait state generated
1 = wait state generated

Note: This wait state is to sync Z80 with FDC chip during FDC operation.

D7 = DDEN *
0 = Single Density enabled (FM)
1 = Double Density enabled (MFM)

Name: DISKOUT *
Port Address: F0 — F3
Access: WRITE ONLY
Description: Output to FDC Control Registers

Port F0 = FDC Command Register

Port F1 = FDC Track Register

Port F2 = FDC Sector Register

Port F3 = FDC Data Register

(Refer to FDC Manual for Bit Assignments)

Name: DISKIN *
Port Address: F0 — F3
Access: READ ONLY
Description: Input FDC Control Registers

Port F0 = FDC Status Register

Port F1 = FDC Track Register

Port F2 = FDC Sector Register

Port F3 = FDC Data Register

(Refer to FDC Manual for Bit Assignment)

Name: MODOUT *
Port Address: EC — EF
Access: WRITE ONLY
Description: Output to Configuration Latch

D0 = (RESERVED)

D1 = CASSMOTORON (Sound enable)
0 = Cassette Motor Off (Sound enabled)
1 = Cassette Motor On (Sound disabled)

D2 = MODSEL
0 = 64 or 80 character mode
1 = 32 or 40 character mode

D3 = ENALTSET
0 = Alternate character set disabled
1 = Alternate character set enabled

D4 = ENEXTIO
0 = External IO Bus disabled
1 = External IO Bus enabled

D5 = (RESERVED)

D6 = FAST
0 = 2 MHZ Mode
1 = 4 MHZ Mode

D7 = (RESERVED)

Name: RTCIN *
Port Address: EC — EF
Access: READ ONLY
Description: Clear Real Time Clock Interrupt

D0 — D7 = DON T CARE

Name: RS232OUT *
Port Address: E8 — EB
Access: WRITE ONLY
Description: UART Control Data Control Modem Control, BRG Control

Port E8 = UART Master Reset

Port E9 = BAUD Rate Gen Register

Port EA = UART Control Register (Modem Control Reg)

Port EB = UART Transmit Holding Reg

(Refer to Model III or 4 Manual for Bit Assignments)

Name: RS232IN *
Port Address: E8 — EB
Access: READ ONLY
Description: Input UART and Modem Status

Port E8 = MODEM STATUS

Port E9 = (RESERVED)

Port EA = UART Status Register

Port EB = UART Receive Holding Register (Resets DR)

(Refer to Model III or 4 Manual for Bit Assignments)

Name: WRNMIMASKREG *
Port Address: E4 — E7
Access: WRITE ONLY
Description: Output NMI Latch

D0 — D5 = (RESERVED)

D6 = ENMOTOROFFINT
0 = Disables Motoroff NMI
1 = Enables Motoroff NMI

D7 = ENINTRQ
0 = Disables INTRQ NMI
1 = Enables INTRQ NMI

Name: RDNMISTATUS *
Port Address: E4 — E7
Access: READ ONLY
Description: Input NMI Status

D0 = 0

D2 — D4 = (RESERVED)

D5 = RESET (not needed)
0 = Reset Asserted (Problem)
1 = Reset Negated

D6 = MOTOROFF
0 = Motoroff Asserted
1 = Motoroff Negated

D7 = INTRQ
0 = INTRQ Asserted
1 = INTRQ Negated

Name: WRINTMASKREG *
Port Address: E0 — E3
Access: WRITE ONLY
Description: Output INT Latch

D0 — D1 = (RESERVED)

D2 = ENRTC
0 = Real time clock interrupt disabled
1 = Real time clock interrupt enabled

D3 = ENIOBUSINT
0 = External IO Bus interrupt disabled
1 = External IO Bus interrupt enabled

D4 = ENXMITINT
0 = RS232 Xmit Holding Reg. empty int. disabled
1 = RS232 Xmit Holding Reg. empty int. enabled

D5 = ENRECINT
0 = RS232 Rec Data Reg. full int. disabled
1 = RS232 Rec. Data Reg. full int enabled

D6 = ENERRORINT
0 = RS232 UART Error interrupts disabled
1 = RS232 UART Error interrupts enabled

D7 = (RESERVED)

Name: RDINTSTATUS *
Port Address: E0 — E3
Access: READ ONLY
Description: Input INT Status

D0 — D1 = (RESERVED)

D2 = RTC INT

D3 = IOBUS INT

D4 = RS232 XMIT INT

D5 = RS232 REC INT

D6 = RS232 UART ERROR INT

D7 = (RESERVED)

Name: BOOT *
Port Address: 9C — 9F
Access: WRITE ONLY
Description: Enable or Disable Boot ROM

D0 = ROM *
0 = Boot ROM Disabled
1 = Boot ROM Enabled

D1 — D7 = (RESERVED)

Name: SEN *
Port Address: 90 — 93
Access: WRITE ONLY
Description: Sound output

D0 = SOUND DATA

D1 — D7 = (RESERVED)

Name: OPREG *
Port Address: 84
Access: WRITE ONLY
Description: Output to operation reg.

D0 = SEL0

D1 = SEL1

SEL1	SEL0	MODE
0	0	0
0	1	1
1	0	2
1	1	3

D2 = 8064
0 = 64 character mode
1 = 80 character mode

D3 = INVERSE
0 = Inverse video disabled
1 = Inverse video enabled

D4 = SRCPAGE — Points to the page to be mapped as new page
0 = U64K, L32K Page
1 = U64K, U32K Page

D5 = ENPAGE — Enables mapping of new page
0 = Page mapping disabled
1 = Page mapping enabled

D6 = DESPAGE — Points to the page where new page is to be mapped
0 = L64K, U32K Page
1 = L64K, L32K Page

D7 = PAGE
0 = Page 0 of Video Memory
1 = Page 1 of Video Memory

3.1.8 Video Circuit

The heart of the video display circuit in the Model 4P is the 68045 Cathode Ray Tube Controller (CRTC), U85 The CRTC is a preprogrammed video controller that provides two screen formats 64 by 16 and 80 by 24 The format is controlled by pin 3 of the CRTC (8064*) The CRTC generates all of the necessary signals required for the video display These signals are VSYNC (Vertical Sync), HSYNC (Horizontal Sync) for proper sync of the monitor, DISPEN (Display Enable) which indicates when video data should be output to the monitor, the refresh memory addresses (MA0-MA13) which addresses the video RAM, and the row addresses (RA0-RA4) which indicates which scan line row is being displayed The CRTC also provides hardware scrolling by writing to the internal Memory Start Address Register by OUTing to Port 88H The internal cursor control of the 68045 is not used in the Model 4P video circuit

Since the 80 by 24 screen requires 1,920 screen memory locations, a 2K by 8 static RAM (U82) is used for the video RAM Addressing to the video RAM (U82) is provided by the 68045 when refreshing the screen and by the CPU when updating of the data is performed These two sets of address lines are multiplexed by three 74LS157s (U83, U84, and U104) The multiplexers are switched by CRTCLK which allows the CRTC to address the video RAM during the high state of CRTCLK and the CPU access during the low state A10 from the CPU is controlled by PAGE* which allows two display pages in the 64 by 16 format When updates to the video RAM are performed by the CPU, the CPU is held in a WAIT state until the CRTC is not addressing the video RAM This operation allows reads and writes to video RAM without causing hashing on the screen The circuit that performs this function is a 74LS244 buffer (U103), an 8 bit transparent latch, 74LS373 (U102) and a Delay line circuit shared with Dynamic RAM timing circuit consisting of a 74LS74 (U95), 74LS32 (U94), 74LS04 (U74), 74LS00 (U96), 74LS02 (U75), and Delay Line (U97) During a CPU Read Access to the Video RAM, the address is decoded by the PAL U109 and asserts VIDEO* low This is inverted by U74 (1/6 of 74LS04) which pulls one input of U96 (1/4 of 74LS00) and in turn asserts VWAIT * low to the CPU RD is high at this time and is latched into U95 (1/2 of 74LS74) on the rising edge of XADR7* XADR7* is inverse of CRTCLK which drives the CRTC (68045), and the address multiplexers U83, U84, and U104

When RD is latched by U95 the Q output goes low releasing WAIT* from the CPU The same signal also is sent to the Delay Line (U97) through U116 (1 4 of 74F08) The Delay line delays the falling edge 240 ns for VLATCH* which latches the read data from the video RAM at U102 The data is latched so the CRTC can refresh the next address location and prevent any hashing MRD* decoded by U108 and a memory read is ORed with VIDEO* which enables the data from U102 to the data bus The CPU then reads the data and completes the cycle A CPU write is slightly more complex in operation As in the RD cycle, VIDEO* is asserted low which asserts VWAIT* low to the CPU WR is high at this time which is NANDed with VIDEO and synced with CRTCLK to create VRAMDIS that disables the video RAM output On the rising edge of XADR7*, WR is latched into U95 (1/2 of 74LS74) which releases VWAIT* and starts cycle through the Delay Line After 30ns DLYVWR* (Delayed video write) is asserted low which also asserts VBUFEN* (Video Buffer Enable) low VBUFEN* enabled data from the Data bus to the video RAM Approximately 120ns later DLYVWR* is negated high which writes the data to the video RAM and negates VBUFEN* turning off buffer The CPU then completes WR cycle to the video RAM Refer to Video RAM CPU Access Timing Figure 5-12 for timing of above RD or WR cycles

During screen refresh, CRTCLK is high allowing the CRTC to address Video RAM The data out of the video RAM is latched by LOAD* into a 74LS273 (U101) D7 is generated by INVERSE* through U125 (1/6 of 74S04), and U123 (1/4 of 74LS08) This decoding determines if character should be alpha-numeric only (if inverse high) or unchanged (INVERSE* low) The outputs of U101 are used as address inputs the character generator ROM (U42) A9 is decoded with ENALTSET (Enable Alternate Set) and Q7 of U101, which resets A9 to a low if Q7 and ENALTSET are high See ENALTSET Control Table below

ENALTSET	Q7	Q6	A9
0	0	0	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

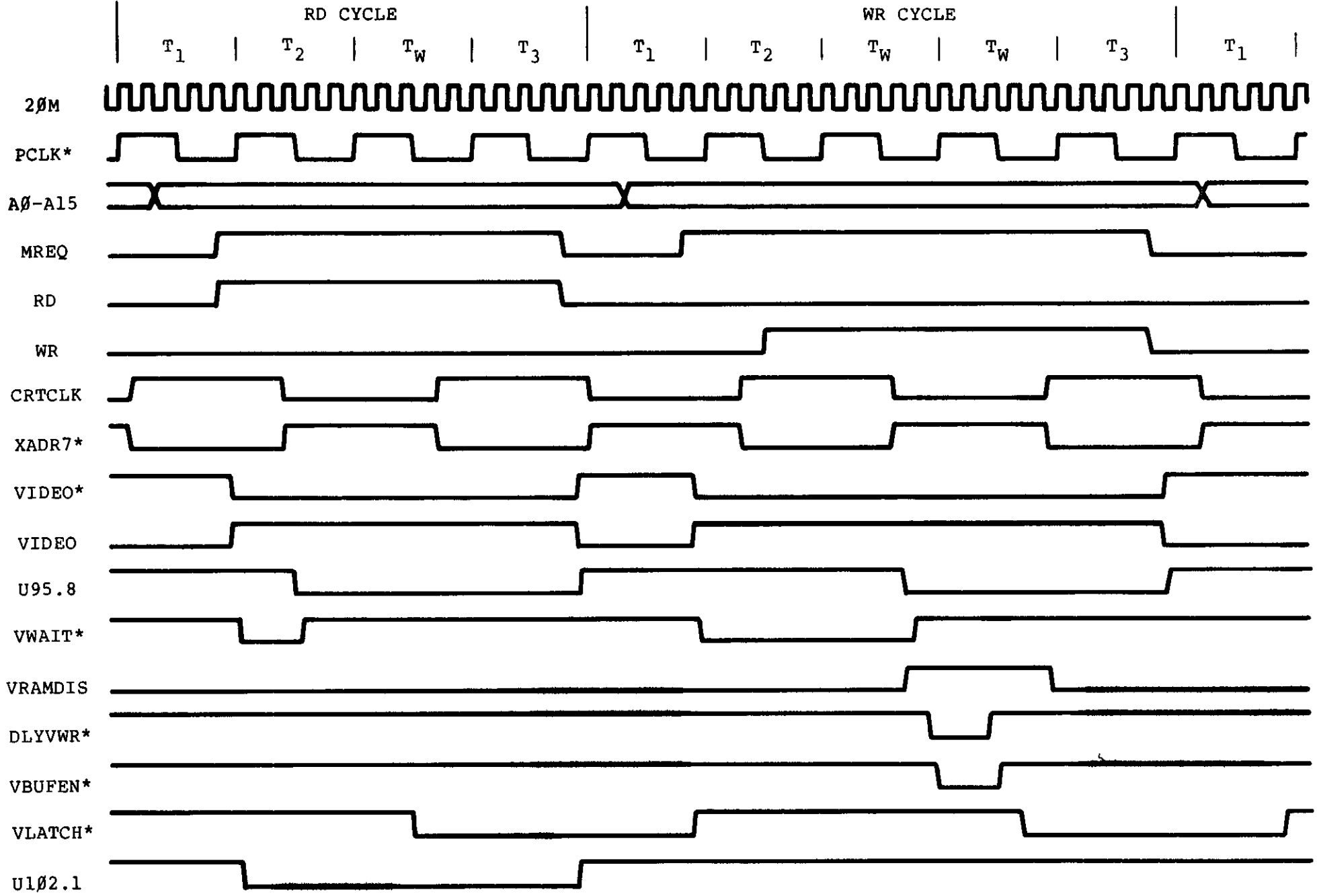


Figure 3-12. Video RAM CPU Access Timing

RA0-RA3 row addresses from the CRTC are used to control which scan line is being displayed The Model 4P has a 4-bit full adder 74LS283 (U61) to modify the Row address During a character display DLYGRAPHIC* is high which applies a high to all 4 bits to be added to row address This will result in subtracting one from Row address count and allow all characters to be displayed one scan line lower The purpose is so inverse characters will appear within the inverse block When a graphic block is displayed DLYGRAPHIC* is low which causes the row address to be unmodified Moving jumper from E14-E15 to E15-E16 will disable this circuit

DLYCHAR* and DLYGRAPHICS are inverse signals and control which data is to be loaded into the shift register U63 When DLYCHAR* is low and DLYGRAPHIC* is high, the Character Generator ROM (U42) is enabled to output data when DLYCHAR* is high and DLYGRAPHIC* is low the graphics characters from U41 (74LS15) is buffered by U43 (74LS244) to the shift register The data is loaded into the shift register on the rising edge of SHIFT* when LOADS* is low Blanking is accomplished by masking off LOADS* so no data will be loaded and zero data will be shifted out with the serial input of U63, pin 1, grounded Serial video data is output U63 pin 13 and is mixed with inverse and/or hires graphics information by (1/4 or 74LS86) U143 The video data is then mixed with a DO7 Rate clock, either DOT* and DCLK, to create distinct dots on the monitor DOT* and DCLK are inverse signals and are provided to allow a choice to obtain the best video results The video information is filtered by F34, R45 (47 ohm resistor), and C241 (100 pf Cap) and output to video monitor VSYNC and HSYNC are buffered by (1/2 of 74LS86) U143 and are also output to video monitor Refer to Video Circuit Timing Figure 3-13, Video Blanking Timing Figure 3-14, and Inverse Video Timing Figure 3-15 for timing relationships of Video Circuit

3.1.9 Keyboard

The keyboard interface of the Model 4P consists of open collector drivers which drive an 8 by 8 key matrix keyboard and an inverting buffer which buffers the key or keys pressed on the data bus The open collector drivers (U56 and U57 (7416) are driven by address lines A0-A7 which drive the column lines of the keyboard matrix The ROW lines of the keyboard are pulled up by a 1 5 kohm resistor pack RP2 The ROW lines are buffered and inverted onto the data bus by U58 (74LS240) which is enabled when KEYBD* is a logic low KEYBD* is a memory mapped decode of addresses 3800-3BFF in Model III Mode and F400-F7FF in Model 4/4P mode Refer to the Memory Map under Address Decode for more information During real time operation, the CPU will scan the keyboard periodically to check if any keys are pressed If no key is pressed, the resistor pack RP2 keeps the inputs of U58 at a logic high U58 inverts the data to a logic low and buffers it to the data bus which is read by the CPU If a key is pressed when the CPU scans the correct column line, the key pressed will pull the corresponding row to a logic low U58 inverts the signal to a logic high which is read by the CPU

3.1.10 Real Time Clock

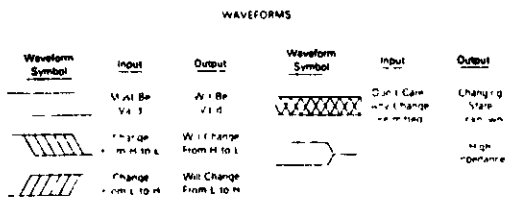
The Real Time Clock circuit in the Model 4P provides a 30 Hz (in the 2 MHz CPU mode) or 60 Hz (in the 4 MHz CPU mode) interrupt to the CPU By counting the number of interrupts that have occurred, the CPU can keep track of the time The 60 Hz vertical sync signal (VSYNC) from the video circuitry is used for the Real Time Clock s reference In the 2 MHz mode, FAST is a logic low which sets the Preset input, pin 4 of U22 (74LS74), to a logic high This allows the 60 Hz (VSYNC) to be divided by 2 to 30 Hz The output of 1/2 of U22 is ORed with the original 60 Hz and then clocks another 74LS74 (1/2 of U22) If the real time clock is enabled (ENRTC at a logic high), the interrupt is latched and pulls the INT* line low to the CPU When the CPU recognizes the interrupt, the pulse is counted and the latch reset by pulling RTCIN* low In the 4 MHz mode, FAST is a logic high which keeps the first half of U22 in a preset state (the Q* output at a logic low) The 60 Hz is used to clock the interrupts

NOTE: If interrupts are disabled, the accuracy of the real time clock will suffer

3.1.11 Line Printer Port

The Line Printer Port Interface consists of a pulse generator, an eight-bit latch, and a status line buffer The status of the line printer is read by the CPU by enabling buffer U3 (74LS244) This buffer is enabled by LPRD* which is a memory map and port map decode In Model III mode, only the status can be read from memory location 37E8 or 37E9 The status can be read in all modes by an input from ports F8-FB For a listing of the bit status, refer to Port Map section

After the printer driver software determines that the printer is ready for printing (by reading the correct status), the characters to be printed are output to Port F8-FB U2, a 74LS374 eight-bit latch, latches the character byte and outputs to the line printer One-half of U1 (74LS123), a one-shot, is then triggered which generates an appropriate strobe signal to the printer which signifies a valid character is ready The output of the one-shot is buffered by 1/6th of the U21 (74LS04) to prevent noise from the printer cable from flase-triggering the one-shot



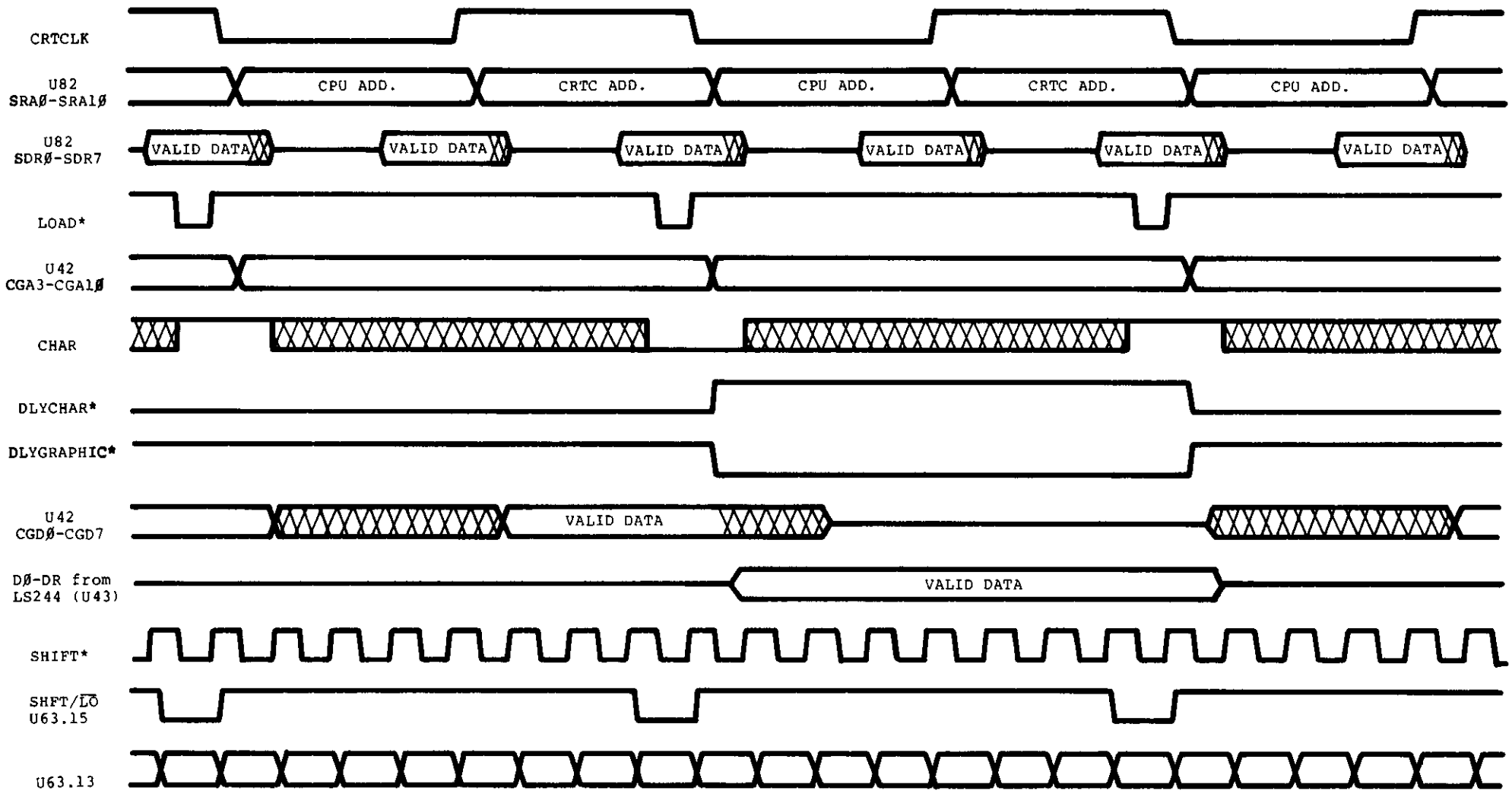


Figure 3-13. Video Circuit Timing

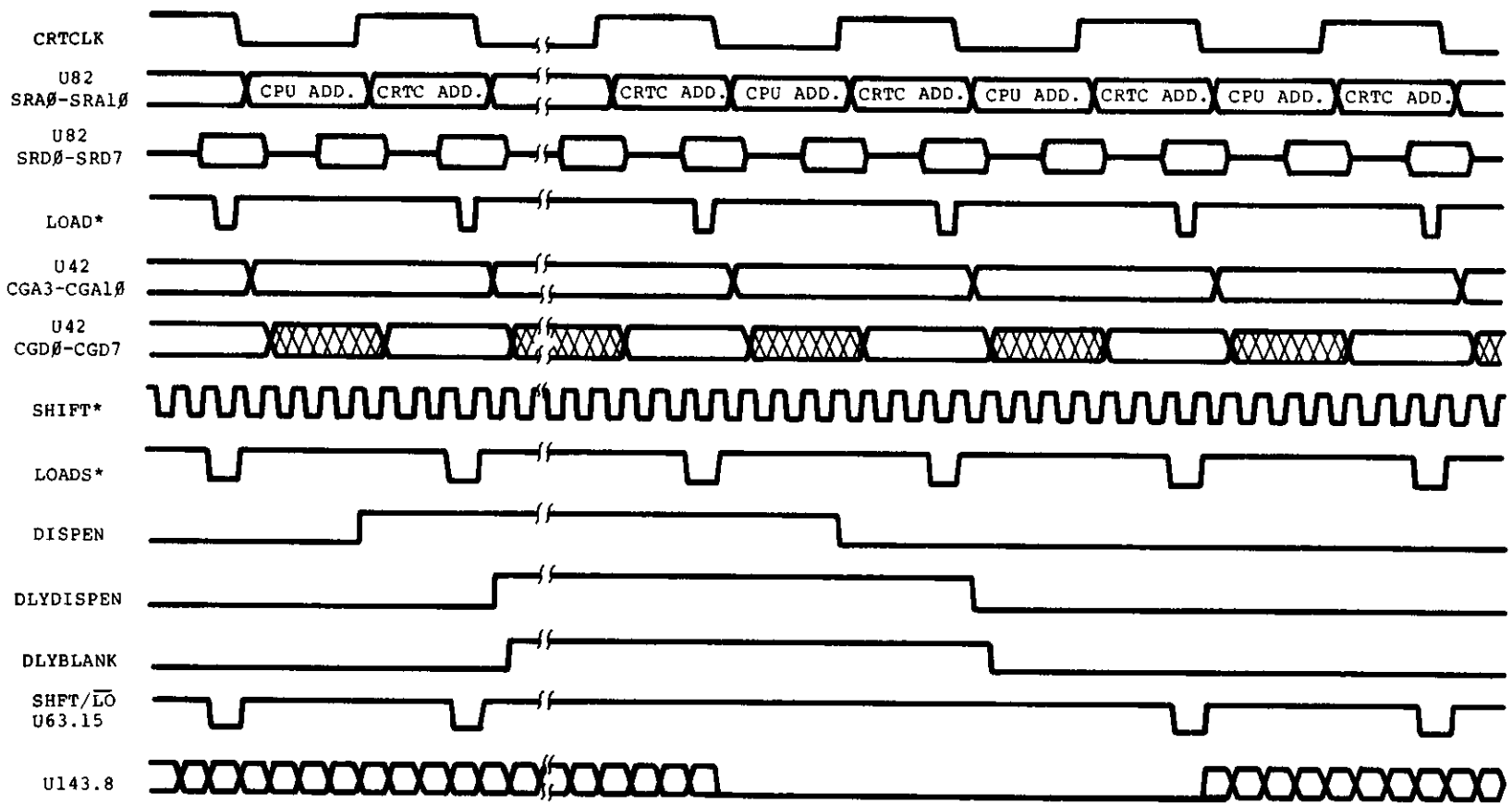


Figure 3-14. Video Blanking Timing

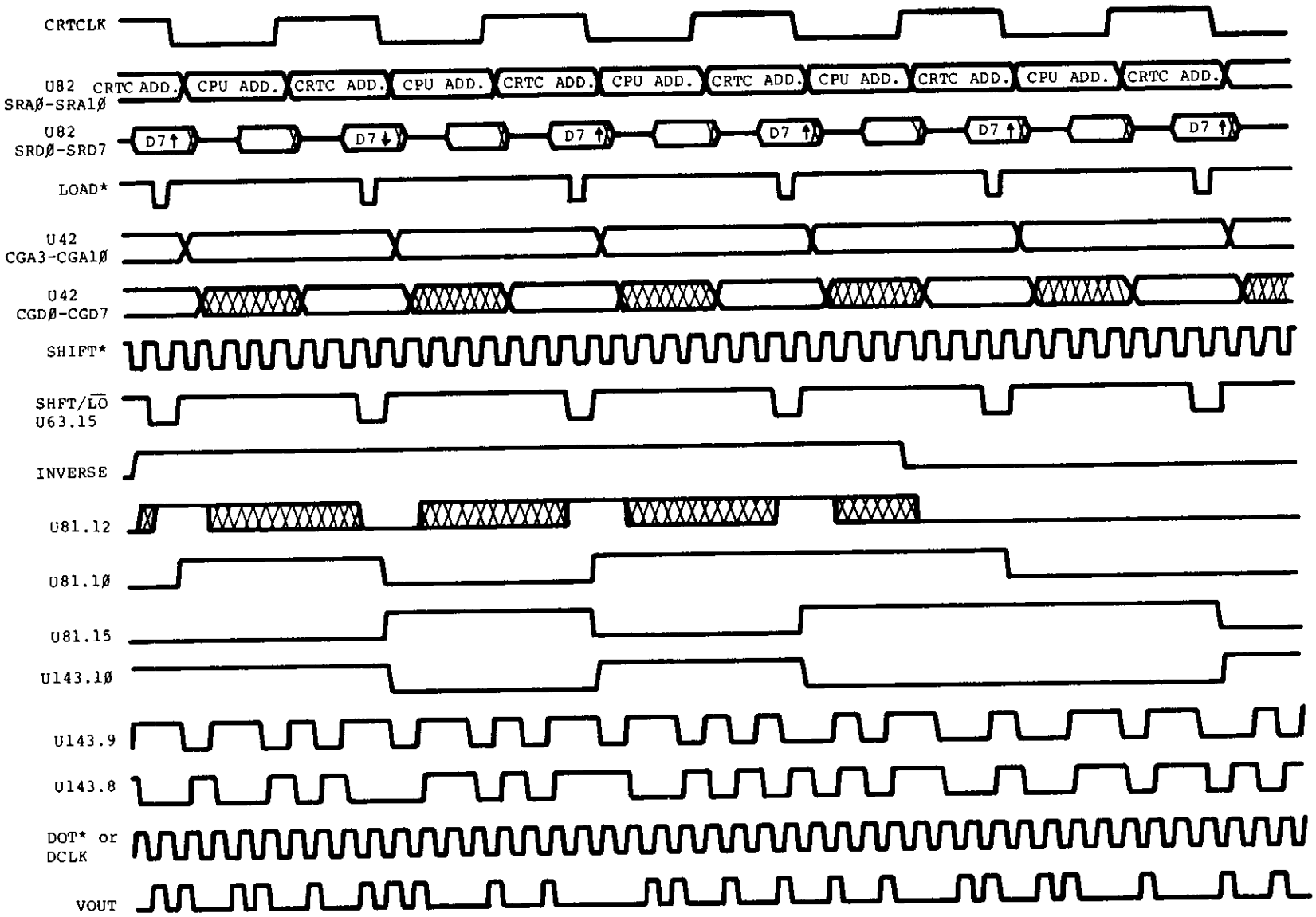


Figure 3-15. Inverse Video Timing

3.1.12 Graphics Port

The Graphics Port (J7) on the Model 4P is provided to attach the optional Graphics Board The port provides D0-D7 (Data Lines), A0-A3 (Address Lines), IN*, GEN* and RESET* for the necessary interface signals for the Graphics Board GEN* is generated by negative ORing Port selects GSEL0* (8C-8FH) and GSEL1* (80-83H) together by (1 4 of 74LS08) U23 The resulting signal is negative ANDed with IORQ* by (1 4 of 74S32) U62 Seven timing signals are provided to allow synchronization of Main Logic Board Video and Graphics Board Video These timing signals are VSYNC, HSYNC, DISPEN, DCLK, H, I, and J Three control signals from the Graphics Board are used to sync to CPU access and select different video modes WAIT* controls the CPU access by causing the CPU to WAIT till video is in retrace area before allowing any writes or reads to Graphics Board RAM ENGRAF is asserted when Graphics video is displayed ENGRAF also disables inverse video mode on Main Logic Board Video CL166* (Clear 74L166) is used to enable or disable mixing of Main Logic Board Video and Graphics Board Video If CL166* is negated high, then mixing is allowed in all for video modes 80 x 24, 40 x 24, 64 x 16, and 32 x 16. If CL166* is asserted low, this will clear the video shift register U63, which allows no video from the Main Logic Board In this state 8064* is automatically asserted low to put screen in 80 x 24 video mode Refer to Figure 3-16 Graphic Board Video Timing for timing relationships Refer to the Model 4/ 4P Graphics Board Service information for service or technical information on the Graphics Board

3.1.13 Sound

The sound circuit in the Model 4P is compatible with the Sound Board which was optional in the Model 4 Sound is generated by alternately setting and clearing data bit D0 during an OUT to port 90H The state of D0 is latched by U130 (1/2 of a 74LS74) and the output is amplified by Q2 which drives a piezoelectric sound transducer The speed of the software loop determines the frequency, and thus, the pitch of the resulting tone Since the Model 4P does not have a cassette circuit, some existing software that used the cassette output for sound would have been lost The Model 4P routes the cassette latch to the sound board through U142 When the CASSMOTORON signal is a logic low, the cassette motor is off, then the cassette output is sent to the sound circuit

3.1.14 I/O Bus Port

The Model 4P Bus is designed to allow easy and convenient interfacing of I/O devices to the Model 4P The I O Bus supports all the signals necessary to implement a device compatible with the Z80s I/O structure

Addresses

A0 to A7 allow selection of up to 256* input and 256 output devices if external I O is enabled

*Ports 80H to 0FFH are reserved for System use

Data

DB0 to DB7 allow transfer of 8-bit data onto the processor data bus is external I O is enabled

Control Lines

1 M1* — Z80A signal specifying an M1 or Operation Code Fetch Cycle or with IOREQ*, it specifies an Interrupt acknowledge

2 IN* — Z80A signal specifying than an input is in progress Logic AND of IOREQ* and WR*

3 OUT* — Z80A signal specifying that an output is in progress Logic AND of IOREQ* and WR*

4 IOREQ* — Z80A signal specifying that an input or output is in progress or with M1*, it specifies an interrupt acknowledge

5 RESET* — system reset signal

6 IOBUSINT* — input to the CPU signaling an interrupt from an I/O Bus device if I/O Bus interrupts are enabled.

7 IOBUSWAIT* — input to the CPU wait line allowing I/O Bus device to force wait states on the Z80 if external I/O is enabled

8 EXTIOSEL* — input to I/O Bus Port circuit which switches the I/O Bus data bus transceiver and allows and INPUT instruction to read I/O Bus data

The address line, data line, and all control lines except RESET* are enabled only when the ENEXIO bit in port EC is set to one

To enable I/O interrupts, the ENIOBUSINT bit in the PORT E0 (output port) must be a one However, even if it is disabled from generating interrupts, the status of the IOBUSINT* line can still read on the appropriate bit of CPU IOPORT E0 (input port)

See Model 4P Port Bit assignments for port 0FF, 0EC, and 0E0

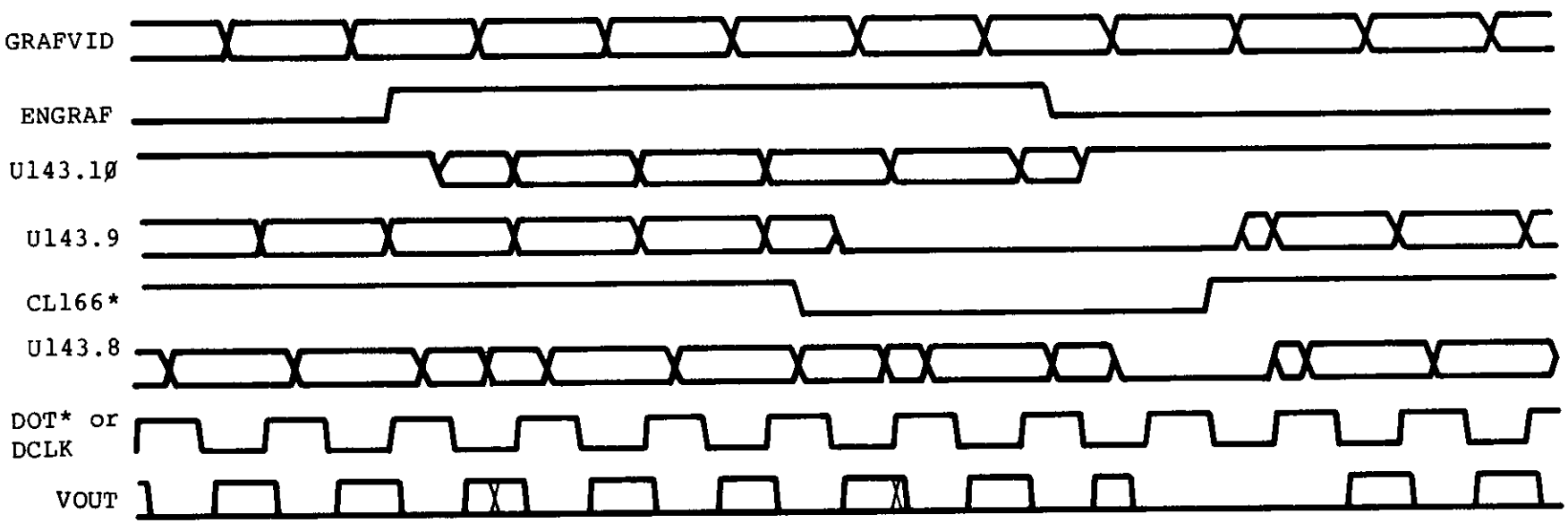


Figure 3-16. Graphic Board Video Timing

The Model 4P CPU board is fully protected from foreign I O devices in that all the I O Bus signals are buffered and can be disabled under software control To attach and use and I O device on the I O Bus certain requirements (both hardware and software) must be met

For input port device use, you must enable external I/O devices by writing to port 0ECH with bit 4 on in the user software. This will enable the data bus address lines and control signals to the I/O Bus edge connector. When the input device is selected, the hardware should acknowledge by asserting EXTIOSEL* low. This switches the data bus transceiver and allows the CPU to read the contents of the I/O Bus data lines. See Figure 3-17 for the timing. EXTIOSEL* can be generated by NANDing IN and the I/O port address.

Output port device use is the same as the input port device in use, in that the external I/O devices must be enabled by writing to port 0ECH with bit 4 on in the user software — in the same fashion

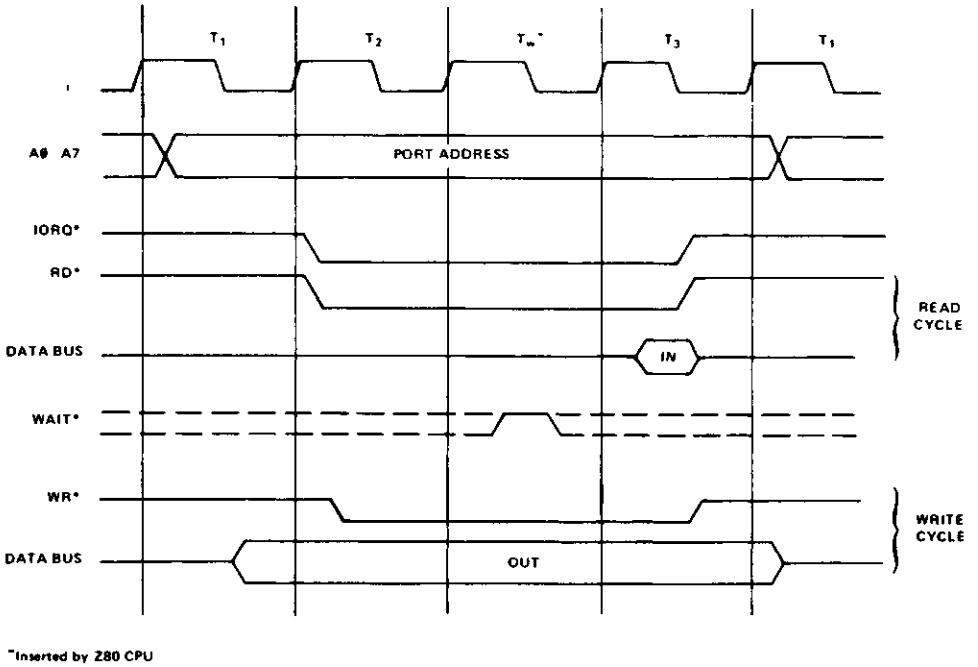
For either input or output devices, the IOBUSWAIT* control line can be used in the normal way for synchronizing slow devices to the CPU Note that since dynamic memories are used in the Model 4P, the wait line should be used with caution Holding the CPU in a wait state for 2 msec or more may cause loss of memory contents since refresh is inhibited during this time It is recommended that the IOBUSWAIT* line be held active no more than 500 µsec with a 25% duty cycle

The Model 4P will support Z80 Mode 1 interrupts A RAM jump table is supported by the LEVEL II BASIC ROMs image and the user must supply the address of his interrupt service routine by writing this address to locations 403E and 403F When an interrupt occurs, the program will be vectored to the user-supplied address if I/O Bus interrupts have been enabled To enable I/O Bus interrupts, the user must set bit 3 of Port 0E0H

3.1.15 FDC Circuit

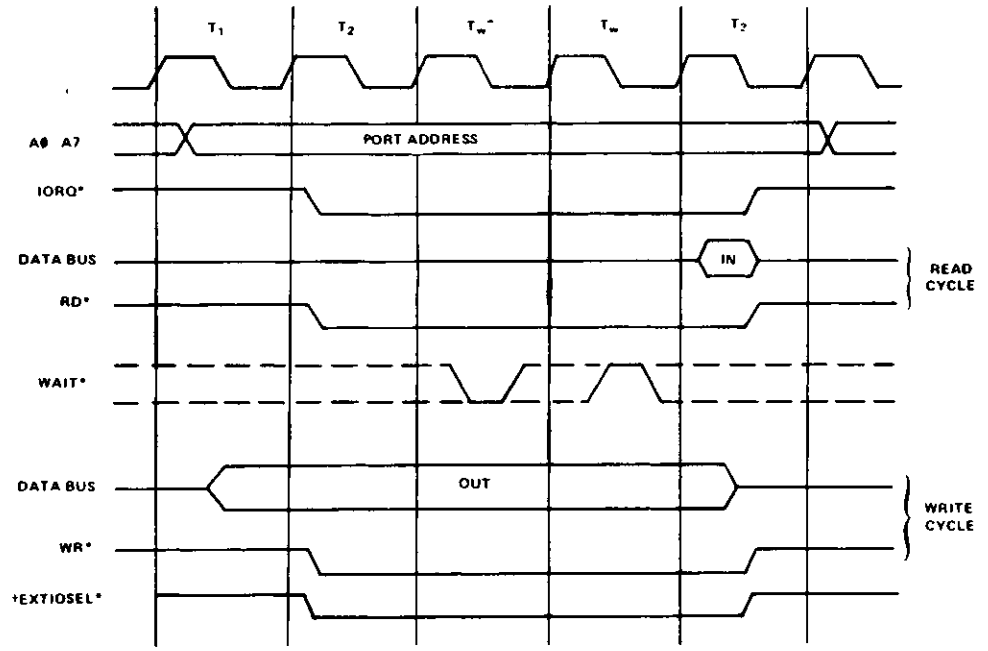
The TRS-80 Model 4P Floppy Disk Interface provices a standard 5-1 4" floppy disk controller The Floppy Disk Interface supports both single and double density encoding schemes Write precompensation can be software enabled or disabled beginning at any track, although the system software enables write precompensation for all tracks greater than twenty-one The amount of write precompensation is 250 nsec and is not adjustable The data clock recovery logic incorporates a digital data separator which achieves state-of-the-art reliability One or two drives may be controlled by the interface All data transfers are accomplished by CPU data requests In double density operation, data transfers are synchronized to the CPU by forcing a wait to the CPU and clearing the wait by a data request from the FDC chip The end of the data transfer is indicated by generation of a non-maskable interrupt from the interrupt request output of the FDC chip A hardware watchdog timer insures that any error condition will not hang the wait line to the CPU for a period long enough to destroy RAM contents

Input or Output Cycles.



*Inserted by Z80 CPU

Input or Output Cycles with Wait States.



*Inserted by Z80 CPU

+Coincident with IORQ* only on INPUT cycle

Figure 3-17. I/O Bus Timing Diagram

Control and Data Buffering

The Floppy Disk Controller Board is an I O port-mapped device which utilizes ports E4H F0H F1H F2H F3H and F4H The decoding logic is implemented on the CPU board (Refer to Paragraph 5 1 5 Address Decoding for more information on Port Map) U31 is a bi-directional 8-bit transceiver used to buffer data to and from the FDC and RS-232 circuits The direction of data transfer is controlled by the combination of control signals DISKIN* and RS232IN* If either signal is active (logic low) U31 is enabled to drive data onto the CPU data bus If both signals are inactive (logic high), U31 is enabled to receive data from the CPU board data bus A second buffer (U12) is used to buffer the FDC chip data to the FDC RS232 Data Bus (BD0-BD7). U12 is enabled all the time and it s direction controlled by DISKIN* Again, if DISKIN* is active (logic low) data is enabled to drive from the FDC chip to the Main Data Busses If DISKIN* is inactive (logic high) data is enabled to be transferred to the FDC chip

Nonmaskable Interrupt Logic

Dual D flip-flop U100 (74LS74) is used to latch data bits D6 and D7 on the rising edge of the control signal WRNMIMASKREG* The outputs of U100 enable the conditions which will generate a non-maskable interrupt to the CPU The NMI interrupt conditions which are programmed by doing an OUT instruction to port E4H with the appropriate bits set If data bit 7 is set, an FDC interrupt is enabled to generate an NMI interrupt If data bit 7 is reset interrupt requests request from the FDC are disabled If data bit 6 is set a Motor Time Out is enabled to generate an NMI interrupt If data bit 6 is reset interrupts on Motor Time Out are disabled An IN instruction from port E4H enables the CPU to determine the source of the non-maskable interrupt Data bit 7 indicates the status of FDC interrupt request (INTRQ) (0 = true 1 – false) Data bit 6 indicates the status of Motor Time Out (0 – true, 1 – false) Data bit 5 indicates the status of the Reset signal (0 – true, 1 – false) The control signal RDNMISTATUS* gates this status onto the CPU data bus when active (logic low)

Drive Select Latch and Motor ON Logic

Selecting a drive prior to disk I O operation is accomplished by doing an OUT instruction to port F4H with the proper bit set The following table describes the bit allocation of the Drive Select Latch

Data Bit	Function
D0	Selects Drive 0 when set*
D1	Selects Drive 1 when set*
D2	Selects Drive 2 when set*
D3	Selects Drive 3 when set*
D4	Selects Side 0 when reset Selects Side 1 when set
D5	Write precompensation enabled when set disabled when reset
D6	Generates WAIT if set
D7	Selects MFM mode if set Selects FM mode if reset

*Only one of these bits should be set per output

Hex D flip-flop U32 (74L174) latches the drive select bits side select and FM* MFM bits on the rising edge of the control signal DRVSEL* A dual D flip-flop (U98) is used to latch the Wait Enable and Write precompensation enable bits on the rising edge of DRVSEL* The rising edge of DRVSEL* also triggers a one-shot (1 2 of U54 74LS123) which produces a Motor On to the disk drives The duration of the Motor On signal is approximately three seconds The spindle motors are not designed for continuous operation Therefore, the inactive state of the Motor On signal is used to clear the Drive Select Latch, which de-selects any drives which were previously selected The Motor On one-shot is retriggerable by simply executing another OUT instruction to the Drive Select Latch

Wait State Generation and WAITIMOUT Logic

As previously mentioned, a wait state to the CPU can be initiated by an OUT to the Drive Select Latch with D6 set Pin 5 of U98 will go high after this operation This signal is inverted by 1 4th of U79 and is routed to the CPU where it forces the Z80A into a wait state The Z80A will remain in the wait state as long as WAIT* is low Once initiated, the WAIT* will remain low until one of five conditions is satisfied One half of U77 (a five input NOR gate) is used to perform this function INTQ DRQ, RESET, CLRWAIT, and WAITIMOUT are the inputs to the NOR gate If any one of these inputs is active (logic high) the output of the NOR gate (U77 pin 5) will go low This output is tied to the clear input of the wait latch When this signal goes low, it will clear the Q output (U98 pin 5) and set the Q* output (U98 pin 6) This condition causes WAIT* to go high which allows the Z80 to exit the wait state U99 is a 12-bit binary counter which serves as a watchdog timer to insure that a wait condition will not persist long enough to destroy dynamic RAM contents The counter is clocked by a 1 MHz clock and is enabled to count when its reset pin is low (U99 pin 11) A logic high on U99 pin 11 resets the counter outputs U99 pin 15 is a divide-by-1024 output and is used to generate the signal WAITIMOUT This watchdog timer logic will limit the duration of a wait to 1024μsec, even if the FDC chip should fail to generate a DRQ or an INTRQ

If an OUT to Drive Select Latch is initiated with D6 reset (logic low), a WAIT is still generated The 12-bit binary counter will count to 2 which will output CLRWAIT and clear the WAIT state This allows the WAIT to occur only during the OUT instruction to prevent violating any Dynamic RAM parameters

NOTE: This automatic WAIT will cause a 1-2 μsec wait each time an out to Drive Select Latch is performed

Clock Generation Logic

A 4 MHz crystal oscillator and a 4-bit binary counter are used to generate the clock signals required by the FDC board The 4 MHz oscillator is implemented with two inverters (1 3 of U39) and a quartz crystal (Y2) The output of the oscillator is inverted and buffered by 1 6 of U39 to generate a TTL level square wave signal U37 is a 4-bit binary counter which is divided into a divide-by-2 and a divide-by-8 section The divide-by-2 section is used to generate the 2 MHz output at pin 12 The 2 MHz is NANDed with 4MHz by 1 4 of U19 and the output is used to clock the divide-by-8 section of U37 A 1 MHz clock is generated at pin 9 of U37 which is 90 phase-shifted from the 2 MHz clock This phase relationship is used to gate the guaranteed Write Data Pulse (WD) to the Write precompensation circuit The 4 MHz is used to clock the digital data separator U18 and the Write precompensation shift register U55 The 1 MHz clock is used to drive the clock input of the FDC chip (U13) and the clock input of the watchdog timer (U99)

Disk Bus Output Drivers

High current open collector drivers U20 and U56 are used to buffer the output signals from the FDC circuit to the disk drives

Write Precompensation and Write Data Pulse Shaping Logic

The Write Precompensation logic is comprised of U55 (74LS195) 1 4 of U19 (74LS00) 1 4 of U74 (74LS04) and 1 2 of U77 (74LS260) U55 is a parallel in serial out shift register and is clocked by 4 MHz which generates a precompensation value of 250 nsec The output signals EARLY and LATE of the FDC chip (U13) are input to P0 and P2 of the shift register A third signal is generated by 1 4 of U75 when neither EARLY nor LATE is active low and is input to P1 of U55 WD of the FDC chip is NANDed with 2 MHz to gate the guaranteed Write Data Pulse to U55 for the parallel load signal SHFT LD When U55 pin 9 is active low the signals preset at P1-P3 are clocked in on the rising edge of the 4 MHz clock After U55 pin 9 goes high the data is shifted out at a 250 nsec rate EARLY will generate a 250 nsec delay NOT EARLY AND NOT LATE will generate a 500 nsec delay and LATE will generate a 750 nsec delay This provides the necessary precompensation for the write data As mentioned previously Write Precompensation is enabled through software by an OUT to the Drive Select Latch with bit 5 set This sets the Q output of the 74LS74 (U98 pin 9) which is ANDed with DDEN which disables the shift register U55 DDEN disables Write Precompensation in the single density mode The resulting signal also enables U75 to allow the write data (WD) to bypass the Write Precompensation circuit The Write Data (WD) pulse is shaped by a one-shot (1 2 of U54) which stretches the data pulses to approximately 500 nsec

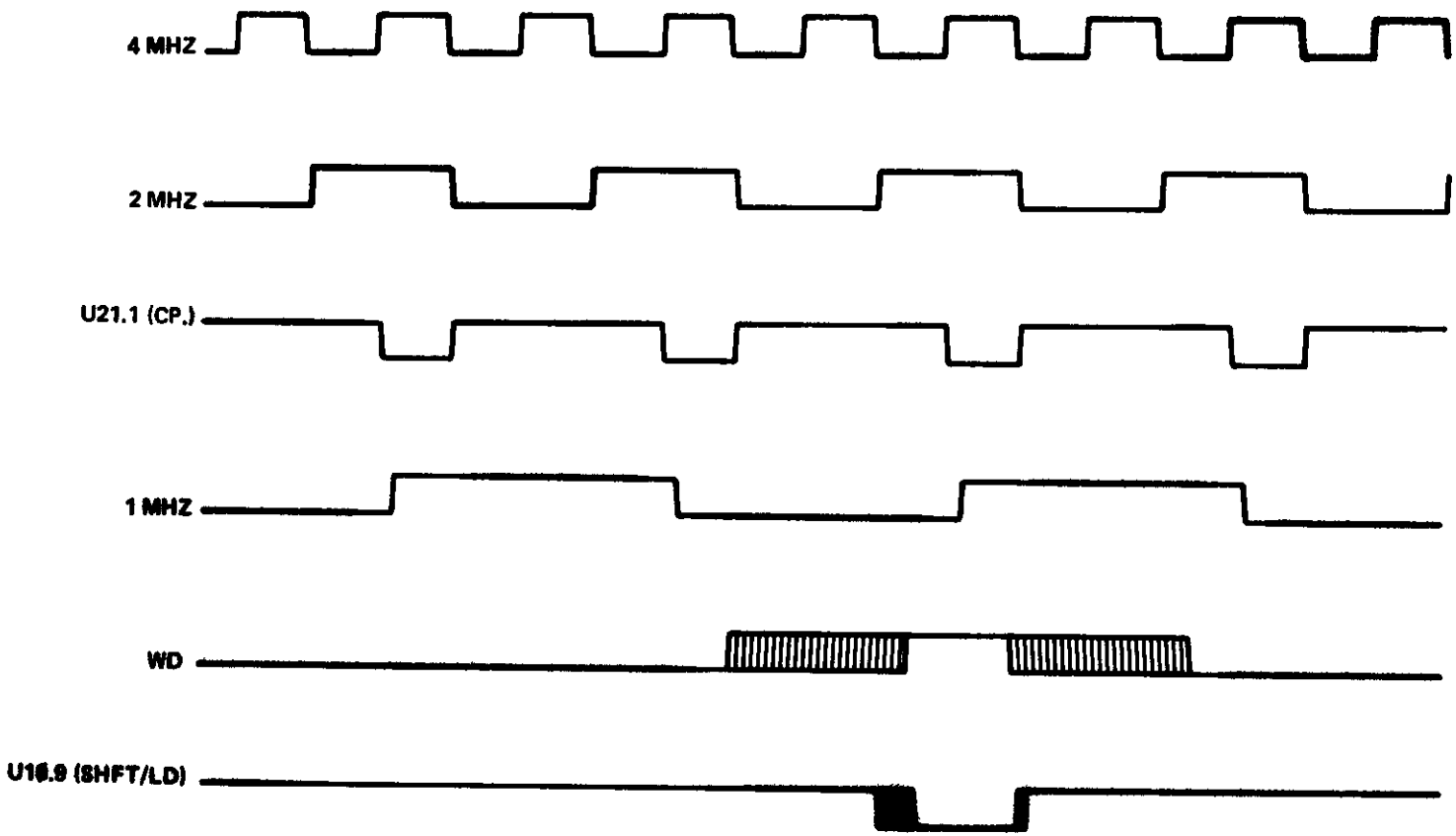


Figure 3-18. Write Precompensation Timing

Clock and Read Data Recovery Logic

The Clock and Read Data Recovery Logic is comprised of one chip U18 (FDC9216) The FDC9216 is a Floppy Disk Data Separator (FDDS) which converts a single stream of pulses from the disk drive into separate clock and data pulses for input to the FDC chip The FDDS consists of a clock divider a long-term timing corrector a short-time timing corrector and reclocking circuitry The reference clock (REFCLK) is a 4 MHz and is divided by the internal clock divider CD0 and CD1 of the FDDS chip control the divisor which divides REFCLK With DC1 grounded (logic low), CD0 (when a logic low) generates a divide-by-1 for MFM mode and when logic high generates a divide-by-2 for FM mode CD0 is controlled by the signal DDEN* which is Double Density enable or MFM enable The FDDS detects the leading edges of RD* pulses and adjusts the phase of the internal clock to generate the separated clock (SEPCLK) to the FDC chip The separate long and short term timing correctors assure the clock separation to be accurate The separated Data (SEPD*) is used as the RDD* input to the FDC chip

Floppy Disk Controller Chip

The 1793 is an MOS LSI device which performs the functions of a floppy disk formatter/controller in a single chip implementation The following port addresses are assigned to the internal registers of the 1793 FDC chip

Port No.	Function
F0H	Command Status Register
F1H	Track Register
F2H	Sector Register
F3H	Data Register

3.1.16 RS-232-C Circuit

RS-232C Technical Description

The RS-232C circuit for the Model 4P computer supports asynchronous serial transmissions and conforms to the EIA RS-232C standards at the input-output interface connector (J4) The heart of the circuit is the TR1865 Asynchronous Receiver Transmitter U30 It performs the job of converting the parallel byte data from the CPU to a serial data stream including start stop, and parity bits For a more detailed description of how this LSI circuit performs these functions refer to the TR1865 data sheets and application notes The transmit and receive clock rates that the TR1865 needs are supplied by the Baud Rate Generator U52 (BR1941L) or (BR1943) This circuit takes the 5 0688 MHz supplied by the system timing circuit and the programmed information received from the CPU over the data bus and divides the basic clock rate to provide two clocks The rates available from the BRG go from 50 Baud to 19200 Baud See the BRG table for the complete list

BRG Programming Table

Nibble Loaded	Transmit Receive Baud Rate	16X Clock	Supported by SETCOM
0H	50	0 8 kHz	Yes
1H	75	1 2 kHz	Yes
2H	110	1 76 kHz	Yes
3H	134 5	2 1523 kHz	Yes
4H	150	2 4 kHz	Yes
5H	300	4 8 kHz	Yes
6H	600	9 6 kHz	Yes
7H	1200	19 2 kHz	Yes
8H	1800	28 8 kHz	Yes
9H	2000	32 081 kHz	Yes
AH	2400	38 4 kHz	Yes
BH	3600	57 6 kHz	Yes
CH	4800	76 8 kHz	Yes
DH	7200	115 2 kHz	Yes
EH	9600	153 6 kHz	Yes
FH	19200	307 2 kHz	Yes

The RS-232C circuit is port mapped and the ports used are E8 to EB Following is a description of each port on both input and output

Port	Input	Output
E8	Modem status	Master Reset, enables UART control register load
EA	UART status	UART control register load and modem control
E9	Not Used	Baud rate register load enable bit
EB	Receiver Holding register	Transmitter Holding register

Interrupts are supported in the RS-232C circuit by the Interrupt mask register (U92) and the Status register (U44) which allow the CPU to see which kind of interrupt has occurred Interrupts can be generated on receiver data register full, transmitter register empty, and any one of the errors — parity, framing, or data overrun This allows a minimum of CPU overhead in transferring data to or from the UART The interrupt mask register is port E0 (write) and the interrupt status register is port E0 (read) Refer to the IO Port description for a full breakdown of all interrupts and their bit positions

All Model I, III, and 4 software written for the RS-232-C interface is compatible with the Model 4P RS-232-C circuit, provided the software does not use the sense switches to configure the interface. The programmer can get around this problem by directly programming the BRG and UART for the desired configuration or by using the SETCOM command of the disk operating system to configure the interface . The TRS-80 RS-232C Interface hardware manual has a good discussion of the RS-232C standard and specific programming examples (Catalog Number 26-1145).

Pinout Listing

The following list is a pinout description of the DB-25 connector (P1).

Pin No.	Signal
1	PGND (Protective Ground)
2	TD (Transmit Data)
3	RD (Receive Data)
4	RTS (Request to Send)
5	CTS (Clear To Send)
6	DSR (Data Set Ready)
7	SGND (Signal Ground)
8	CD (Carrier Detect)
19	SRTS (Spare Request to Send)
20	DTR (Data Terminal Ready)
22	RI (Ring Indicate)

SECTION IV

4P GATE ARRAY THEORY OF OPERATION

4.2 MODEL 4P GATE ARRAY THEORY OF OPERATION

4.2.1 Introduction

Contained in the following paragraphs is a description of the component parts of the Model 4P CPU Gate Array It is divided into the logical operational functions of the computer All components are located on the Main CPU board inside the case housing Refer to Section 3 for disassembly assembly procedures

4.2.2 Reset Circuit

The Model 4P reset circuit provides the neccessary reset pulses to all circuits during power up and reset operations R25 and C214 provide a time constant which holds the input of U121 low during power-up This allows power to be stable to all circuits before the RESET* and RESET signals are applied When C214 charges to a logic high, the output of U121 triggers the input of a retriggerable one-shot multivibrator (U1) U1 outputs a pulse with an approximate width of 70 microsecs When the reset switch is pressed on the front panel, this discharges C214 and holds the input of U121 low until the switch is released On release of the switch, C214 again charges up triggering U121 and U1 to reset the microcomputer Another signal POWRST* is generated to clear drive select circuit immediately when reset switch is pressed

4.2.3 CPU

The central processing unit (CPU) of the Model 4P microcomputer is a Z80A microprocessor The Z80A is capable of running in either 2 MHz or 4 MHz mode The CPU controls all functions of the microcomputer through use of its address lines (A0-A15), data lines (D0-D7), and control lines (/M1, IOREQ RD, WR, /MREQ, and /RFSH) The address lines (A0-A15) are buffered to other ICs through two 74LS244s (U67 and U27) which are enabled all the time with their enables pulled to GND The control lines are buffered to other ICs through a 74F04 (U87) The data lines (D0-D7) are buffered through a bi-directional 74LS245 (U86) which is enabled by BUSEN* and the direction is controlled by BUSDIR*

4.2.4 System Timing

The main timing reference of the microcomputer, with the exception of the FDC circuit, is generated by a Gate Array U148 and a 20 2752 MHz Crystal This reference is internally divided in the Gate Array to generate all necessary timing for the CPU, video circuit, and RS-232-C circuit The CPU clock is generated U148 which can be either 2 or 4MHz depending on the logic state of FAST input (pin 6 of U148) If FAST is a logic low, the U148 generates a 2 02752 MHz clock If FAST is a logic high U148 generates a 4 05504 MHz signal PCLK (pin 23 of U148) is filtered through a ferrite bead (FB2) and 22Ω Resistor (R9) and then fed to the CPU U45 PCLK is generated as a symmetrical clock and is never allowed to be short cycled (eg) Not allowed to generate a low or high pulse under 110 nanoseconds

4.2.4.1 Video Timing

The video timing is also generated by U148 with the help of a PLL Multiplier Module (PMM) U146 These two ICs generate all the necessary timing signals for the four video modes 64 x 16, 32 x 16 80 x 24 and 40 x 24 Two reference clocks are required for the four video modes One reference clock is 10 1376 MHz It is generated internally to U148, and is used by the 64 x 16 and 32 x 16 modes The second reference clock is a 12 672 MHz (12M) clock which is generated by the PMM U146 12M clock is used by the 80 x 24 and 40 x 24 modes A 1 2672 MHz (1 2M16) signal is output from pin 3 of U148 and is generated from the master reference clock, the 20 2752 MHz crystal 1 2M16 is used for a reference clock for the PMM The PMM is internally set to oscillate at 12 672 MHz which is output as 12M U148 divides 12M by 10 to generate a second 1 2672 MHz clock (1 2M10) which is fed into pin 5 of U146 (PMM) The two 1 2672 MHz signals are internally compared in the PMM where it corrects the 12 672 MHz output so it is synchronized with the 20 2752 MHz clock

MODSEL and 8064* signals are used to select the desired video mode 8064* controls which reference clock is used by U127 and MODSEL controls the single or double character width mode Refer to the following chart for selecting each video mode

8064*	MODSEL	Video Mode
0	0	64 x 16
0	1	32 x 16
1	0	80 x 24
1	1	40 x 24

*This is the state to be written to latch U85 Signal is inverted before being input to U148

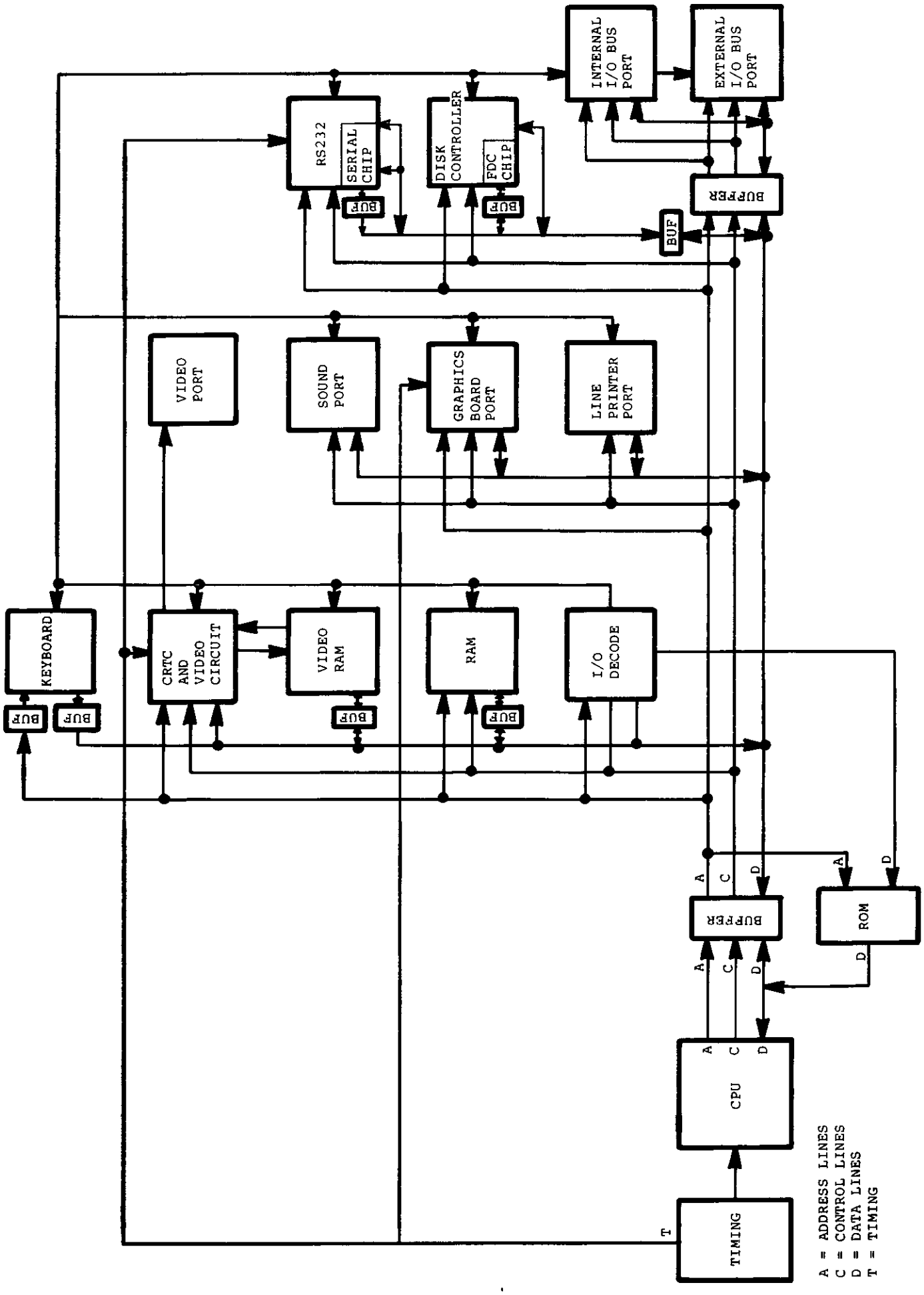


Figure 4-1. Model 4P Functional Block Diagram

DCLK the reference clock selected is output from U148 U148 generates SHIFT* XADR7* CRTCLK LOADS* and LOAD* for proper timing for the four video modes U149 also generated H I and J which are fed to the Graphics Port J7 for reference timings of Hires graphics video Refer to Video Timing Figs 4-2 and 4-3 for timing reference

4.2.5 Address Decode

The Address Decode section will be divided into two subsec tions Memory Map decoding and Port Map decoding

4.2.5.1 Memory Map Decoding

Memory Map Decoding is accomplished by Gate Array 4 2 (U106) Four memory map modes are available which are com patible with the Model III and Model 4 microcomputers U106 is used for memory map control which also controls page map ping of the 32K RAM pages Refer to Memory Maps below

4.2.5.2 Port Map Decoding

Port Map Decoding is accomplished by Gate Array 4 2 (U106) U106 decodes the low order address (A0 A7) from the CPU and decodes the port being selected The IN* signal allows the CPU to read from a selected port and the OUT* signal allows the CPU to write to the selected port Refer to IO Port Assignment

4.2.6 ROM

The Model 4P contains only a 4K x 8 Boot ROM (U70) This ROM is used only to boot up a Disk Operating System into the RAM memory If Model III operation or DOS is required then the RAM from location 0000-37FFH must be loaded with an image of the Model III or 4 ROM code and then exe cuted A file called MODEL A/III is supplied with the Model 4P which contains the ROM image for proper Model III operation On power-up, the Boot ROM is selected and mapped into location 0000-0FFFH After the Boot Sector or the ROM Image is loaded, the Boot ROM must be mapped out by OUTing to port 9CH with D0 set or by selecting Memory Map modes 2 or 3 In Mode 1 the RAM is write enabled for the full 14K This allows the RAM area mapped where Boot ROM is located to be written to while executing out of the Boot ROM Refer to Memory Maps

The Model 4P Boot ROM contains all the code necessary to initialize hardware detect options selected from the keyboard read a sector from a hard disk or floppy and load a copy of the Model III ROM Image (as mentioned) into the lower 14K of RAM

The firmware is divided into the following routines

- Hardware Initialization
- Keyboard Scanner
- Control
- Floppy and Hard Disk Driver
- Disk Directory Searcher
- File Loader
- Error Handler and Displayer
- RS 232 Boot
- Diagnostic Package

Theory of Operation

This section describes the operation of various routines in the ROM Normally the ROM is not addressable by normal use However there are several routines that are available through fixed calling locations and these may be used by operating sys tems that are booting

On a power up or RESET condition the Z80 s program counter is set to address 0 and the boot ROM is switched in The mem ory map of the system is set to Mode 0 (See Memory Map for details) This will cause the Z80 to fetch instructions from the boot ROM

The Initialization section of the Boot ROM now performs these functions

1 Disables maskable and non maskable interrupts
2 Interrupt mode 1 is selected
3 Programs the CRT Controller
4 Initializes the boot ROM control areas in RAM
5 Sets up a stack pointer
6 Issues a Force Interrupt to the Floppy Disk Controller to abort any current activity
7 Sets the system clock to 4mhz
8 Sets the screen to 64 x 16
9 Disables reverse video and the alternate character sets
10 Tests for key being pressed*
11 Clears all 2K of video memory

* This is a special test If the is being pressed then control is transferred to the diagnostic package in the ROM All other keys are scanned via the Keyboard Scanner

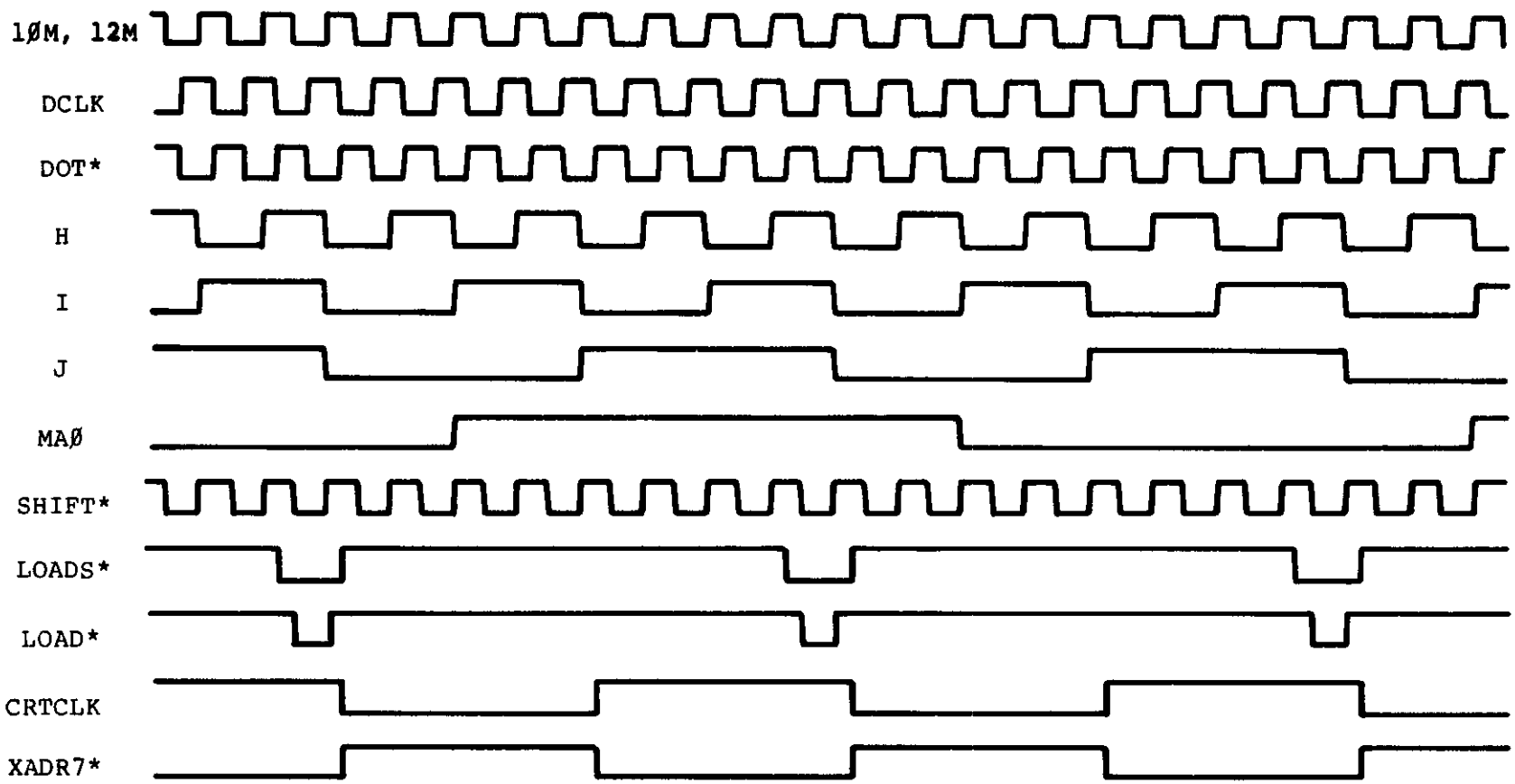


Figure 4-3. Video Timing 32 x 16 Mode 40 x 24 Mode

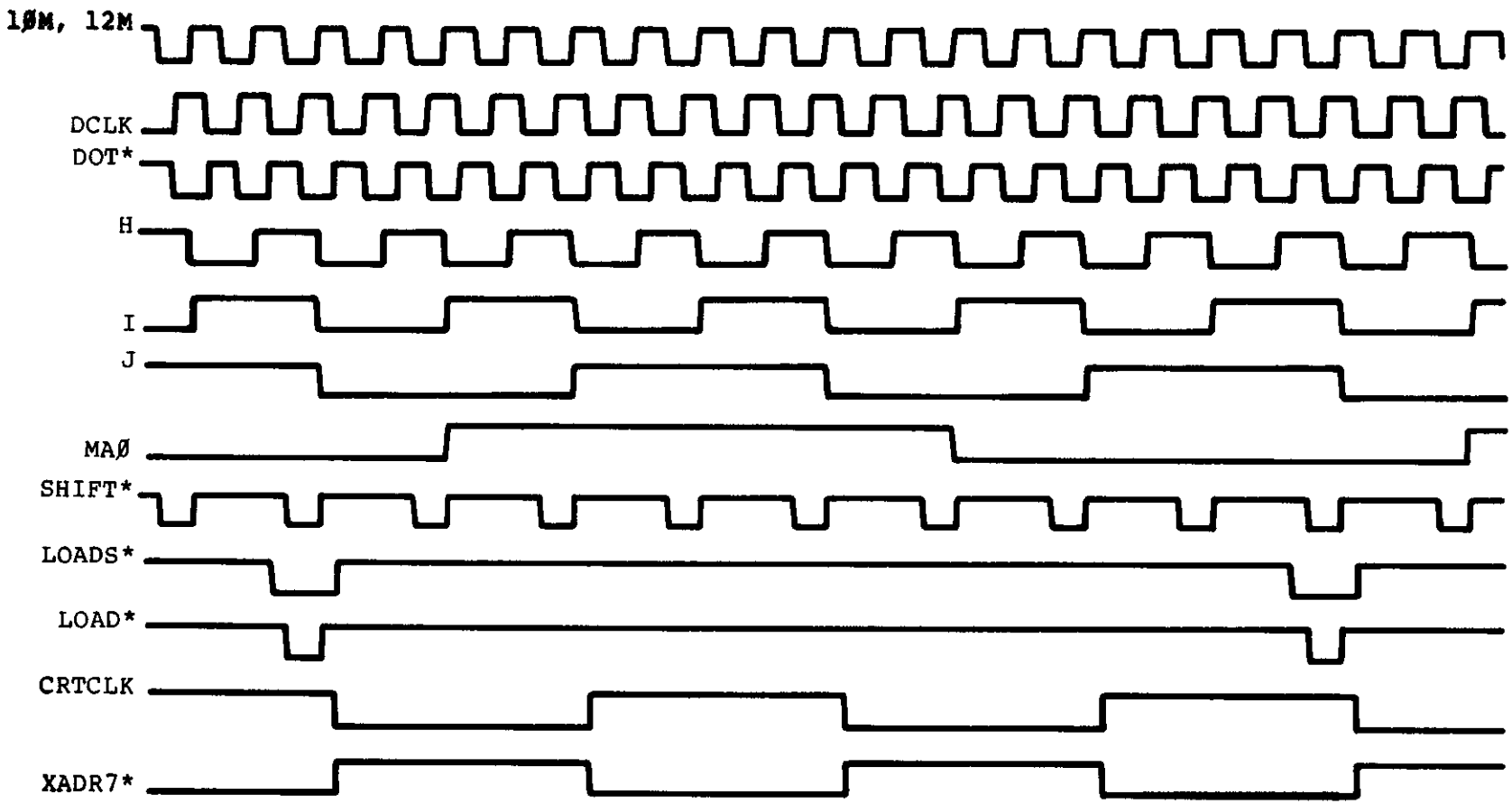


Figure 4-2. Video Timing 64 x 16 Mode 80 x 24 Mode

The Keyboard scanner is now called. It scans the keyboard for a set period of time and returns several parameters based on which, if any, keys were pressed.

The keyboard scanner checks for several different groups of keys. These are shown below:

Function Group	Selection Group
<F1>	A
<F2>	B
<F3>	C
<1>	D
<2>	E
<3>	F
<Left-Shift>	G
<Right-Shift>	
<Ctrl>	
<Caps>	

Special Keys	Misc Keys
<P>	<Enter>
<L>	<Break>
<N>	

When any key in the Function Group is pressed, it is recorded in RAM and will be used by the Control routine in directing the action of the boot. If more than one of these keys are pressed during the keyboard scan, the last one detected will be the one that is used. The Function group keys are currently defined as:

<F1> or <1>	Will cause hard disk boot
<F2> or <2>	Will cause floppy disk boot
<F3> or <3>	Will force Model III mode
<Left-Shift>	Reserved for future use
<Right-Shift>	Boot from RS-232 port
<Ctrl>	Reserved for future use
<Caps>	Reserved for future use

The Special keys are commands to the Control routine which direct handling of the Model III ROM-image. Each key is detected individually.

<P> When loading the Model III ROM-image, the user will be prompted when the disks can be switched or when ROM BASIC can be entered by pressing <Break>.

<N> Instructs the Control routine to not load the Model III ROM-image, even if it appears that the operating system being booted requires it.

<L> Instructs the Control routine to load the Model III ROM-image, even if it is already loaded. This is useful if the ROM-image has been corrupted or when switching ROM-images. (Note that this will not cause the ROM-image to be loaded if the boot sector check indicates that the Model III ROM image is not needed. Press · F3 · or · F3 · and · L · to accomplish that.

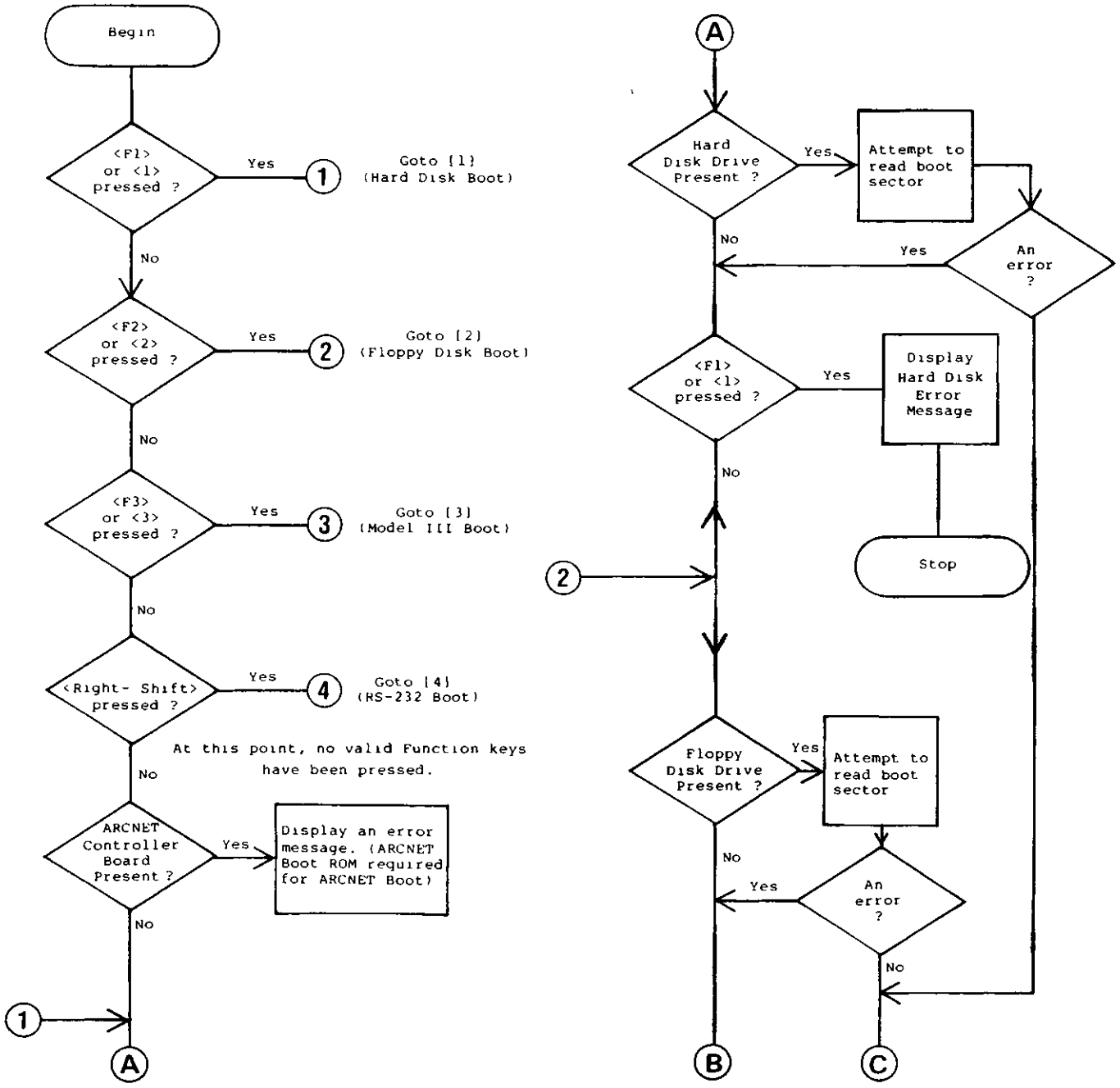
The Selection group keys are used in determining which file will be read from disk when the ROM-image is loaded. For details of this operation, see the Disk Directory Searcher. If more than one of the Selection group keys are pressed, the last one detected will be the one that is used.

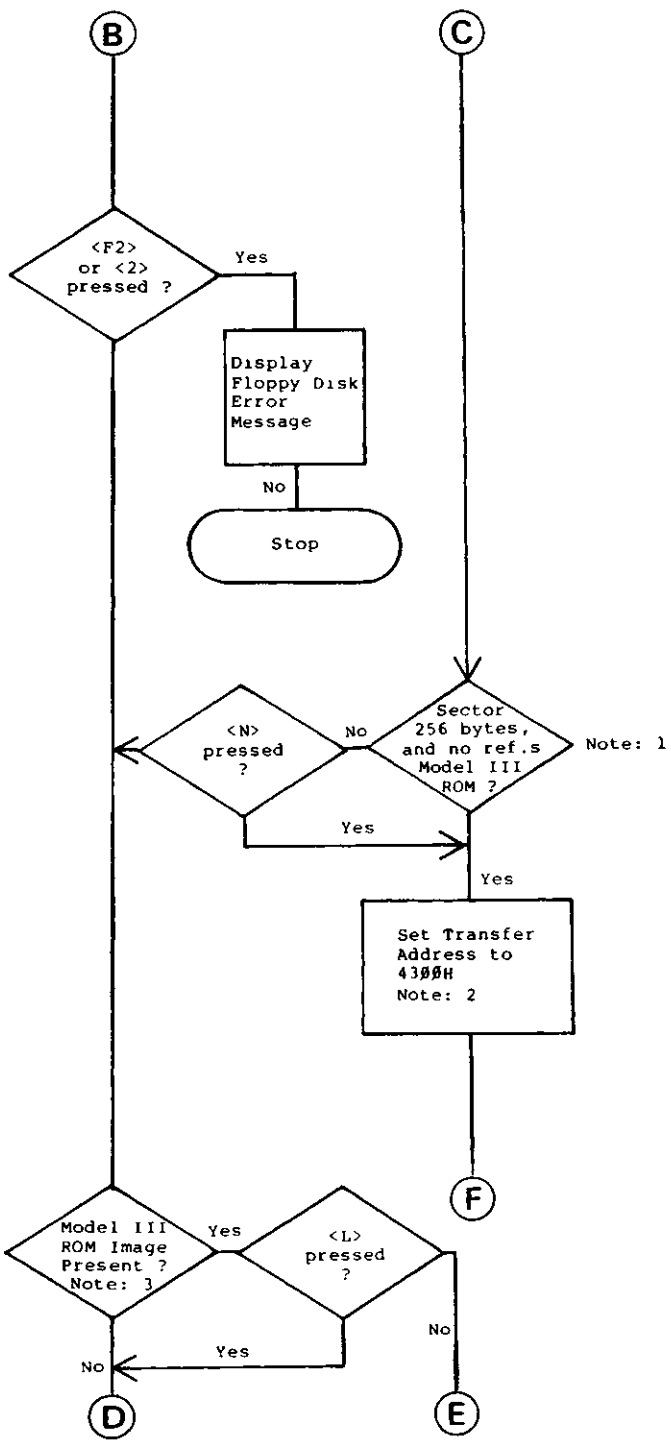
The Miscellaneous keys are:

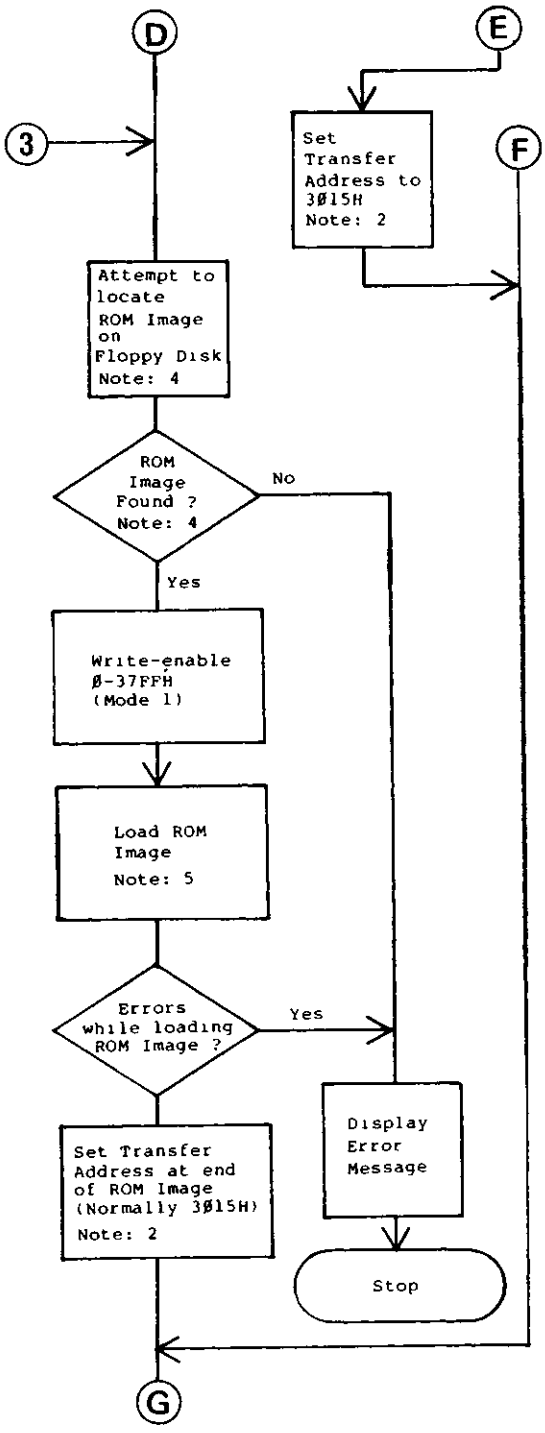
<Break> Pressing this key is simply recorded by setting location 405BH non-zero. It is up to an operating system to use this flag if desired.

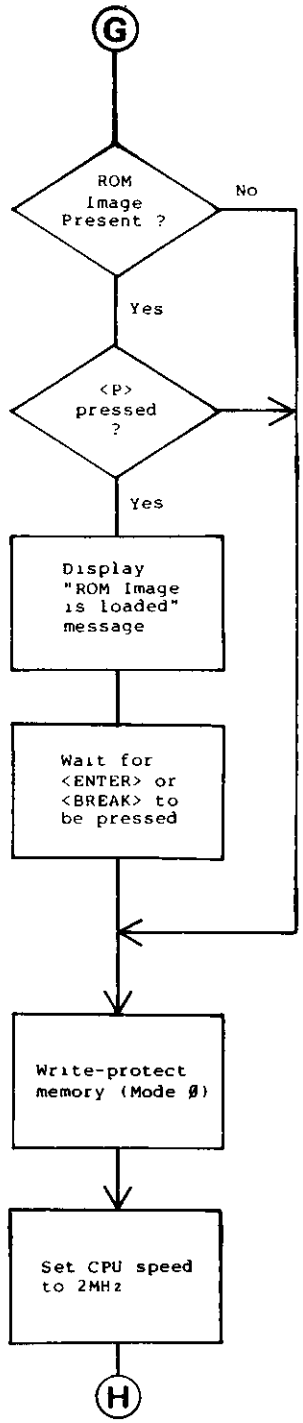
<Enter> Terminates the Keyboard routine. Any other keys pressed up to that time will be acted upon. <Enter> is useful for experienced users who do not want to wait until the keyboard timer expires.

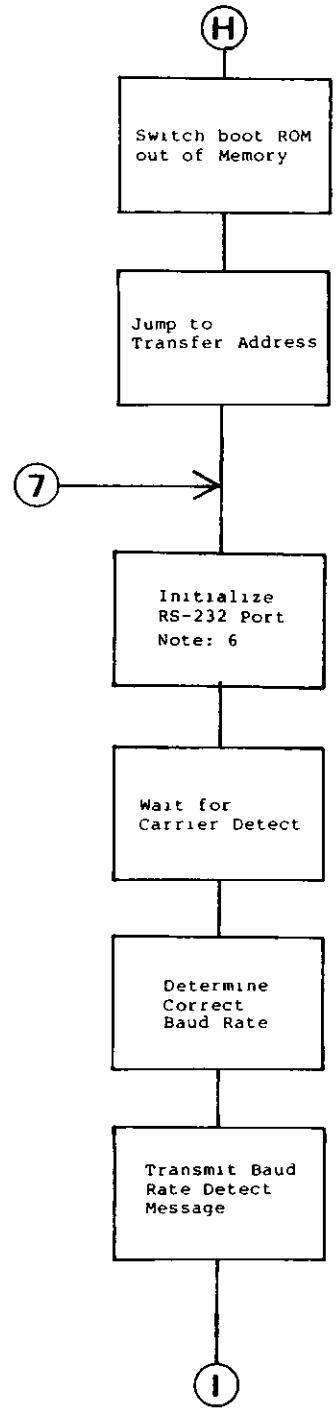
The Control section now takes over and follows the following flowchart.

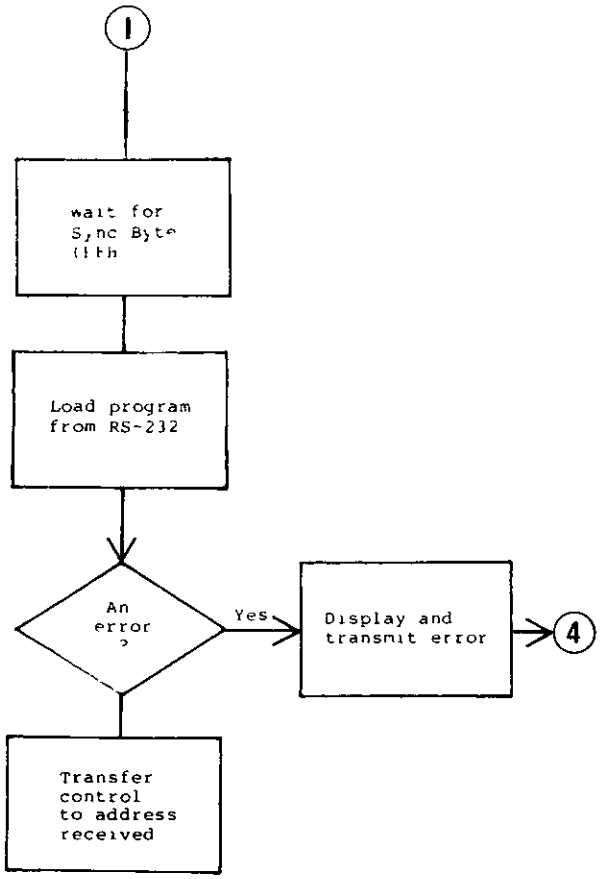

Begin
<F1> or <1> pressed ?
Yes
1
Goto [1] (Hard Disk Boot)
No
<F2> or <2> pressed ?
Yes
2
Goto [2] (Floppy Disk Boot)
No
<F3> or <3> pressed ?
Yes
3
Goto [3] (Model III Boot)
No
<Right- Shift> pressed ?
Yes
4
Goto [4] (RS-232 Boot)
At this point, no valid Function keys have been pressed.
No
ARCNET Controller Board Present ?
Yes
Display an error message. (ARCNET Boot ROM required for ARCNET Boot)
No
1
A
A
Hard Disk Drive Present ?
Yes
Attempt to read boot sector
No
Yes
An error ?
<F1> or <1> pressed ?
Yes
Display Hard Disk Error Message
No
Stop
2
Floppy Disk Drive Present ?
Yes
Attempt to read boot sector
No
Yes
An error ?
No
B
C


B
C
<F2>
or <2>
pressed ?
Yes
Display
Floppy Disk
Error
Message
No
Stop
<N>
pressed
?
No
Sector
256 bytes,
and no ref.s
Model III
ROM ?
Note: 1
Yes
Yes
Set Transfer
Address to
43ØØH
Note: 2
F
Model III
ROM Image
Present ?
Note: 3
Yes
<L>
pressed
?
No
Yes
No
D
E


D
E
3
Set
Transfer
Address to
3Ø15H
Note: 2
F
Attempt to
locate
ROM Image
on
Floppy Disk
Note: 4
ROM
Image
Found ?
Note: 4
No
Yes
Write-enable
Ø-37FFH
(Mode 1)
Load ROM
Image
Note: 5
Errors
while loading
ROM Image ?
Yes
Set Transfer
Address at end
of ROM Image
(Normally 3Ø15H)
Note: 2
Display
Error
Message
Stop
G


G
ROM Image Present ?
No
Yes
<P> pressed ?
Yes
Display "ROM Image is loaded" message
Wait for <ENTER> or <BREAK> to be pressed
Write-protect memory (Mode Ø)
Set CPU speed to 2MHz
H


H
Switch boot ROM out of Memory
Jump to Transfer Address
7
Initialize RS-232 Port
Note: 6
Wait for Carrier Detect
Determine Correct Baud Rate
Transmit Baud Rate Detect Message
I



Notes:

(1) If the boot sector was not 256 bytes in length then it is assumed to be a Model III package and the ROM image will be needed If the sector is 256 bytes in length then the sector is scanned for the sequence CDxx00H The CD is the first byte of a Z80 unconditional subroutine call The next byte can have any value The third byte is tested against a zero What this check does is test for any references to the first 256 bytes of memory All Radio Shack Model III operating systems and many other packages all reference the ROM at some point during the boot sector Most boot sectors will display a message if the system cannot be loaded To save space these routines use the Model III ROM calls to display the message Several ROM calls have their entry points in the first 256 bytes of memory and these references are detected by the boot ROM

Packages that do not reference the Model III ROM in the boot sector can still cause the Model III ROM image to be loaded by coding a CDxx00 somewhere in the boot sector It does not have to be executable At the same time Model 4 packages must take care that there is no sequence of bytes in the boot sector that could be mis-interpreted to be a reference to the Boot ROM An example of this would be sequence 06CD0E00 which is a LD B 0CDH and a LD C 0 If the boot sector cannot be changed then the user must press the F3 key each time the system is started to inform the ROM that the disk contains a Model III package which needs the Model III ROM image

(2) If you are loading a Model 4 operating system then the boot ROM will always transfer control to the first byte of the boot sector, which is at 4300H If you are loading a Model III operating system or about to use Model III ROM BASIC then the transfer address is 3015H This is the address of a jump vector in the C ROM of the Model III ROM image and this will cause the system to behave exactly like a Model III If the ROM image file that is loaded has a different transfer address then that address will be used when loading is complete If the image is already present, the Boot ROM will use 3015H

(3) Two different tests are done to insure that the Model III ROM image is present The first test is to check every third location starting at 3000H for a C3H This is done for 10 locations If any of these locations does not contain a C3H then the ROM image is considered to be not present The next test is to check two bytes at location 000BH If these addresses contain E9E1H then the ROM image is considered to be present

(4) See Disk Director Searcher for more information

(5) See File Loader for more information

(6) The RS-232 loader is described under RS-232 Boot

Disk Directory Searcher

When the Model III ROM image is to be loaded it is always read from the floppy in drive 0

Before the operation begins, some checks are made First the boot sector is read in from the floppy and the first byte is checked to make sure it is either a 00H or a FEH If the byte contains some other value no attempt will be made to read the ROM image from that disk The location of the directory cylinder is then taken from the boot sector and the type of disk is determined This is done by examining the Data Address Mark that

was picked up by the Floppy Disk Controller (FDC) during the read of the sector If the DAM equals 1 the disk is a TRSDOS 1 x style disk If the DAM equals 0 then the disk is a LDOS 5 1 TRSDOS 6 style disk This is important since TRSDOS 1 x disks number sectors starting with 1 and LDOS style disks number sectors starting with 0

Once the disk type has been determined an extra test is made if the disk is a LDOS style disk This test reads the Granule Al location Table (GAT) to determine if the disk is single sided or double sided

The directory is then read one record at a time and a compare is made against the pattern MODEL°₀ for the filename and III for the extension The °₀ means that any character will match this position If the user pressed one of the selection keys (A G) during the keyboard scan then that character is substituted in place of the % character For example if you pressed D then the search would be for the file MODELD with the extension III The searching algorithm searches until it finds the entry or it reaches the end of the directory

Once the entry has been found the extent information for that file is copied into a control block for later use

File Loader

The file loader is actually two modules — the actual loader and a set of routines to fetch bytes from the file on disk The loader is invoked via a RST 28H The byte fetcher is called by the loader using RST 20H Since restart vectors can be re directed the same loader is used by the RS 232 boot The difference is that the RST 20H is redirected to point to the RS 232 data re ceiving routine The loader reads standard loader records and acts upon two types

01 Data Load
1 byte with length of block including address
1 word with address to load the data
n bytes of data where n + 2 equals the length specified

02 Transfer Address
1 byte with the value of 02
1 word with the address to start execution at

Any other loader code is treated as a comment block and is ig nored Once an 02 record has been found the loader stops reading even if there is additional data so be sure to place the 02 record at the end of the file

Floppy and Hard Disk Driver

The disk drivers are entered via RST 8H and will read a sector anywhere on a floppy disk and anywhere on head 1 (top head) in a hard disk drive Either 256 or 512 byte sectors are readable by these routines and they make the determination of the sector size The hard disk driver is compatible with both the WD1000 and the WD1010 controllers The floppy disk driver is written for the WD1793 controller

Serial Loader

Invoking the serial loader is similar to forcing a boot from hard disk or floppy In this case the right shift key must be pressed at some time during the first three seconds after reset The pro gram does not care if the key is pressed forever making it con venient to connect pins 8 and 10 of the keyboard connector with a shorting plug for bench testing of boards This assumes that the object program being loaded does not care about the key closure

Upon entry the program first asserts DTR (J4 pin 20) and RTS (J4 pin 4) true Next Not Ready is printed on the topmost line of the video display Modem status line CD (J4 pin 8) is then sampled The program loops until it finds CD asserted true At that time the message Ready is displayed Then the program sets about determining the baud rate from the host computer

To determine the baud rate the program compares data re ceived by the UART to a test byte equal to 55 hex The receiver is first set to 19200 baud If ten bytes are received which are not equal to the test byte the baud rate is reduced This sequence is repeated until a valid test byte is received If ten failures occur at 50 baud the entire process begins again at 19200 baud If a valid test byte is received the program waits for ten more to ar rive before concluding that it has determined the correct baud rate If at this time an improper byte is received or a receiver er ror (overrun framing or parity) is intercepted the task begins again at 19200 baud

In order to get to this point the host or the modem must assert CD true The host must transmit a sequence of test bytes equal to 55 hex with 8 data bits odd parity and 1 or 2 stop bits The test bytes should be separated by approximately 0 1 second to avoid overrun errors

When the program has determined the baud rate the message

Found Baud Rate x

is displayed on the screen where x is a letter from A to P meaning

A = 50 baud	E = 150	I = 1800	M = 4800
B = 75	F = 300	J = 2000	N = 7200
C = 110	G = 600	K = 2400	O = 9600
D = 134 5	H = 1200	L = 3600	P = 19200

The same message less the character signifying the baud rate is transmitted to the host with the same baud rate and protocol This message is the signal to the host to stop transmitting test bytes

After the program has transmitted the baud rate message it reads from the UART data register in order to clear any overrun error that may have occurred due to the test bytes coming in during the transmission of the message This is because the receiver must be made ready to receive a sync byte signalling the beginning of the command file For this reason it is important that the host wait until the entire baud rate message (16 characters) is received before transmitting the sync byte which is equal to FF hex

When the loader receives the sync byte the message

Loading

is displayed on the screen Again the same message is transmitted to the host and again the host must wait for the entire transmission before starting into the command file

If the receiver should intercept a receive error while waiting for the sync byte the entire operation up to this point is aborted The video display is cleared and the message

Error x

is displayed near the bottom of the screen where x is a letter from B to H meaning

B = parity error
C = framing error
D = parity & framing errors
E = overrun error
F = parity & overrun errors
G = framing & overrun errors
H = parity & framing & overrun errors

The message

Error

is then transmitted to the host The entire process is then repeated from the Not Ready message A six second delay is inserted before reinitialization This is longer than the time required to transmit five bytes at 50 baud so there is no need to be extra careful here

If the sync byte is received without error then the Loading message is transmitted and the program is ready to receive the command file After receiving the Loading message the host can transmit the file without nulls or delays between bytes

(Since the file represents Z80 machine code and all 256 combinations are meaningful it would be disastrous to transmit nulls or other ASCII control codes as fillers acknowledgement or start stop bytes The only control codes needed are the standard command file control bytes)

Data can be transmitted to the loader at 19200 baud with no delays inserted Two stop bits are recommended at high baud rates

See the File Loader description for more information on file loading

If a receive error should occur during file loading the abort procedure described above will take place so when attempting remote control it is wise to monitor the host receiver during transmission of the file When the host is near the object board, as is the case in the factory application or when more than one board is being loaded it may be advantageous or even necessary to ignore the transmitted responses of the object board(s) and to manually pace the test byte sync byte and command file phases of the transmission process using the video display for handshaking

System Programmers Information

The Model 4P Boot ROM uses two areas of RAM while it is running These are 4000H to 40FFH and 4300H to 43FFH (For 512 byte boot sectors the second area is 4300H to 44FFH) If the Model III ROM Image is loaded additional areas are used See the technical reference manual for the system you are using for a list of these areas

Operating systems that want to support a software restart by re-executing the contents of the boot ROM can accomplish this in one of two ways If the operating system relies on the Model III ROM Image then jump to location 0 as you have in the past If the operating system is a Model 4 mode package a simple way is to code the following instructions in your assembly and load them before you want to reset

Absolute Location	Instruction	
0000	DI	
0001	LD	A 1
0003	OUT	(9CH) A

These instructions cause the boot ROM to become addressable After executing the OUT instruction the next instruction executed will be one in the boot ROM (These instructions also exist in the Model III ROM image at location 0) The boot ROM has been written so that the first instruction is at address 0005 The hardware must be in memory mode 0 or 1, or else the boot ROM will not be switched in This operation can be done with an OUT instruction and then a RST 0 can be executed to have the ROM switched in

Restarts can be redirected at any time while the ROM is switched in All restarts jump to fixed locations in RAM and these areas may be changed to point to the routine that is to be executed

Restart	RAM Location	Default Use
0	none	Cold Start Boot
8	4000H	Disk I O Request
10	4003H	Display string
18	4006H	Display block
20	4009H	Byte Fetch (Called by Loader)
28	400CH	File Loader
30	400FH	Keyboard scanner
38	4012H	Reserved for future use
66	4015H	NMI (Floppy I/O Command Complete)

The above routines have fixed entry parameters These are described here

Disk I/O Request (RST 8H)

Accepts

A	1 for floppy, 2 for hard disk
B	Command Initialize 1 Restore 4 Seek 6 Read 12 (All reads have an implied seek)
C	Sector number to read The contents of the location disktype (405CH) are added to this value before an actual read If the disk is a two sided floppy, just add 18 to the sector number
DE	Cylinder number (Only E is used in floppy operations)
HL	Address where data from a read operation is to be stored

Returns

Z	Success, Operation Completed
NZ	Error, Error code in A

Error Codes

3	Hard Disk drive is not ready
4	Floppy disk drive is not ready
5	Hard Disk drive is not available
6	Floppy disk drive is not available
7	Drive Not Ready and no Index (Disk in drive, door open)
8	CRC Error
9	Seek Error
11	Lost Data
12	ID Not Found

Display String (RST 10H)

Accepts

HL	Pointer to text to be displayed Text must be terminated with a null (0)
DE	Offset position on screen where text is to be displayed (A 0000H will be the upper left-hand corner of the display)

Returns
Success Always

A	Altered
DE	Points to next position on video
HL	Points to the null (0)

Display Block (RST 18H)

Accepts

HL	Points to control vector in the format		
	+0	Screen Offset	
	+2	Pointer to text, terminated with null	
	+4	Pointer to text, terminated with null	
	..		
	+n	word FFFFH	End of control vector
or	+n	word FFFEH	Next word is new Screen Offset

If Z flag is set on entry then the first screen offset is read from DE instead of from the control vector

Each string is positioned after the previous string, unless a FFFEH entry is found This is used heavily in the ROM to reduce duplication of words in error messages

Returns
Success Always

DE	Points to next position on video

Byte Fetch (RST 20H)

Accepts None
Returns

Z	Success, byte in A
NZ	Failure, error code in A

Errors

	Any errors from the disk I/O call and
2	ROM Image can't be loaded — Too many extents
10	ROM Image can't be loaded — Disk drive is not ready

File Loader (RST 28H)

Accepts None

Returns

Z	Success
NZ	Failure, error code in A

Errors

	Any errors from the disk I/O call or the byte fetch call and:
0	The ROM image was not found on drive 0

There are several pieces of information left in memory by the boot ROM which are useful to system programmers. These are shown below:

RAM Location	Description
401DH	ROM Image Selected (% for none selected or A-G)
4055H	Boot type 1 = Floppy 2 = Hard disk 3 = ARCNET 4 = RS-232C 5 - 7 = Reserved
4056H	Boot Sector Size (1 for 256, 2 for 512)
4057H	RS-232 Baud Rate (only valid on RS-232 boot)
4059H	Function Key Selected 0 = No function key selected <F1> or <1> 86 <F2> or <2> 87 <F3> or <3> 88 <Caps> 85 <Ctrl> 84 <Left-Shift> 82 <Right-Shift> 83 Reserved 80-81 and 89-90
405BH	Break Key Indication (non-zero if <Break> pressed)
405CH	Disk type (0 for LDOS/ TRSDOS 6,1 for TRSDOS 1.x)

Keep in mind that Model III ROM image will initialize these areas, so this information is useful only to the Model 4 mode programmer.

4.2.7 RAM

Two configurations of Random Access Memory (RAM) are available on the Model 4P: 64K and 128K. The 64K and 128K option use the 6665-type 64K x 1 200NS Dynamic RAM, which requires only a single +5v supply voltage.

The DRAMs require multiplexed incoming address lines. This is accomplished by ICs U110 and U111 which are 74LS157 multiplexers. Data to and from the DRAMs are buffered by a 74LS245 (U118) which is controlled by Gate Array 4.2 (U106). The proper timing signals RAS0*, RAS1*, MUX*, and CAS* are generated by a delay line circuit U94. U116 (1 2 of a 74S112) and U117 (1 4 of a 74F08) are used to generate a precharge circuit. During M1 cycles of the Z80A in 4 MHz mode, the high time in MREQ has a minimum time of 110 nanosecs. The specification of 6665 DRAM requires a minimum of 120 nanosecs so this circuit will shorten the MREQ signal during the M1 cycle. The resulting signal PMREQ is used to start a RAM memory cycle through U114 (a 74S64). Each different cycle is controlled at U114 to maintain a fast M1 cycle so no wait states are required. The output of U114 (PRAS*) is ANDed with RFSH to not allow MUX* and CAS* to be generated during a REFRESH cycle. PRAS* also generates either RAS0* or RAS1*, depending on which bank of RAM the CPU is selecting. GCAS* generated by the delay line U94 is latched by U116 (1 2 of a 74S112) and held to the end of the memory cycle. The output of U116 is ANDed with VIDEO signal to disable the CAS* signal from occurring if the cycle is a video memory access. Refer to M1 Cycle Timing (Figure 4-7 and 4-8), Memory Read and Memory Write Cycle Timing (Figure 4-9) and (Figure 4-10).

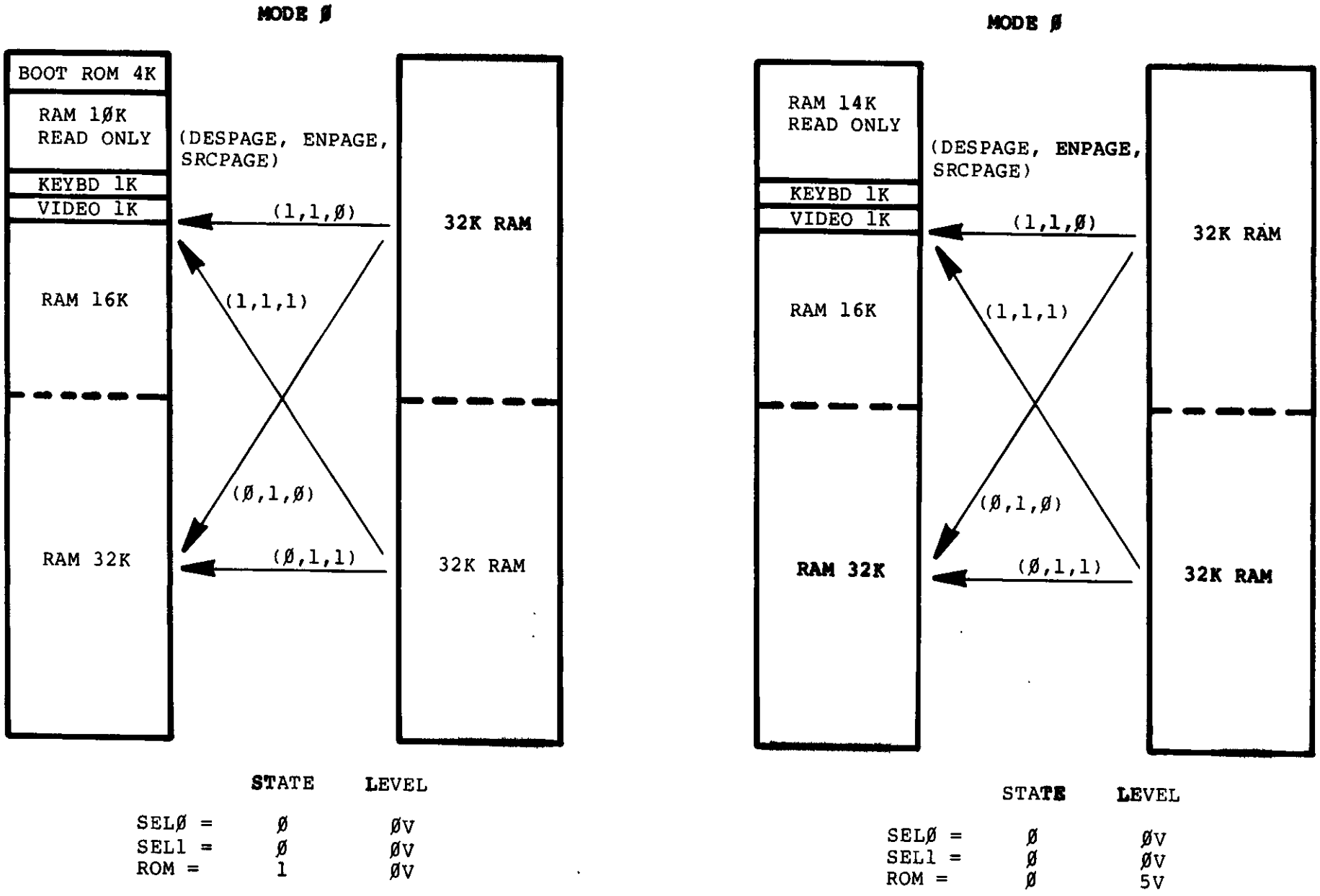
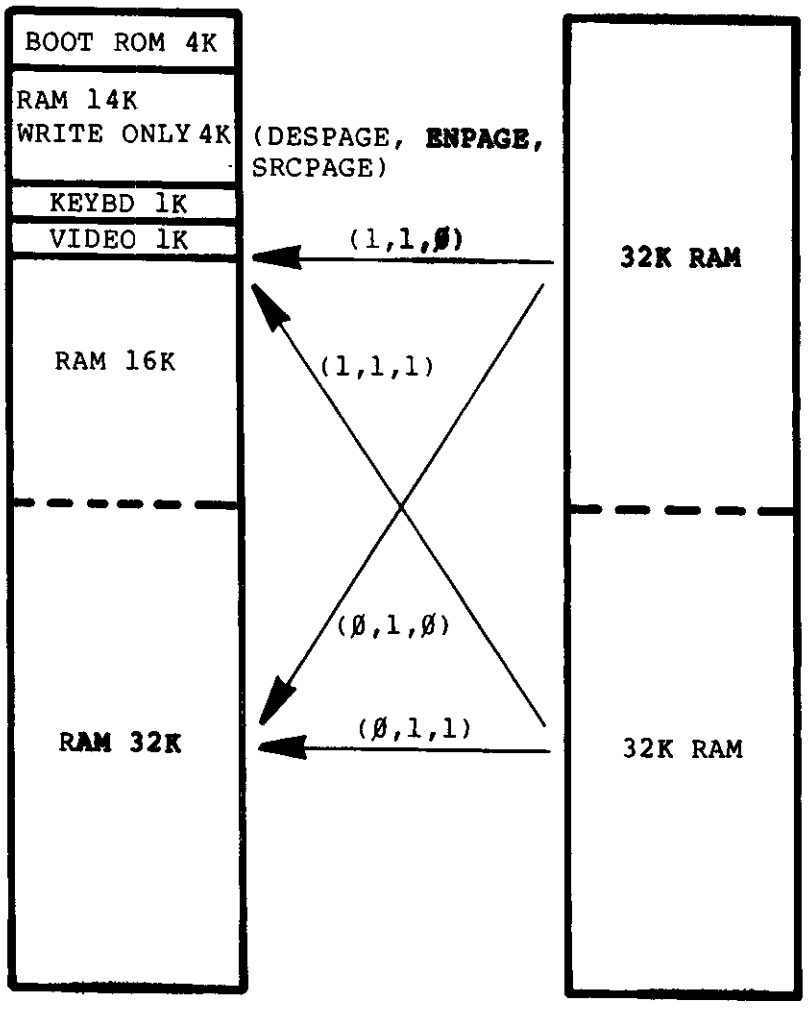


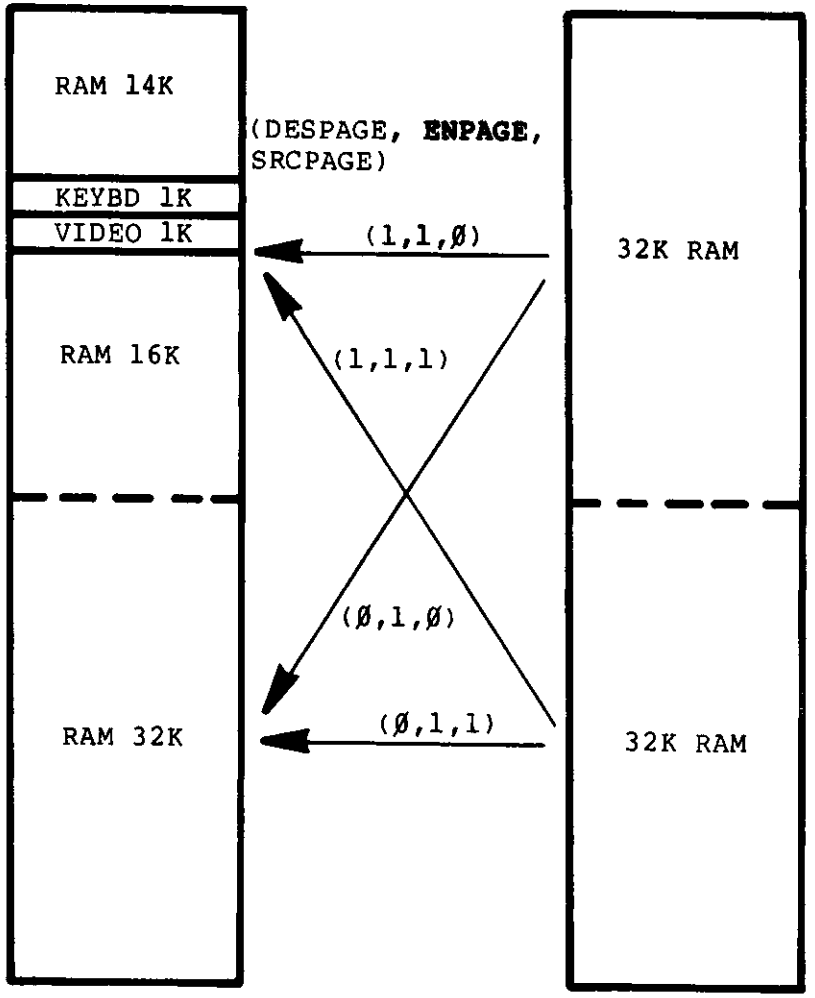
Figure 4-4. Memory

MODE 1



	STATE	LEVEL
SELØ =	1	5V
SEL1 =	Ø	ØV
ROM =	Ø	5V

MODE 1



	STATE	LEVEL
SELØ =	1	5V
SEL1 =	Ø	ØV
ROM =	1	ØV

Figure 4-6. Memory

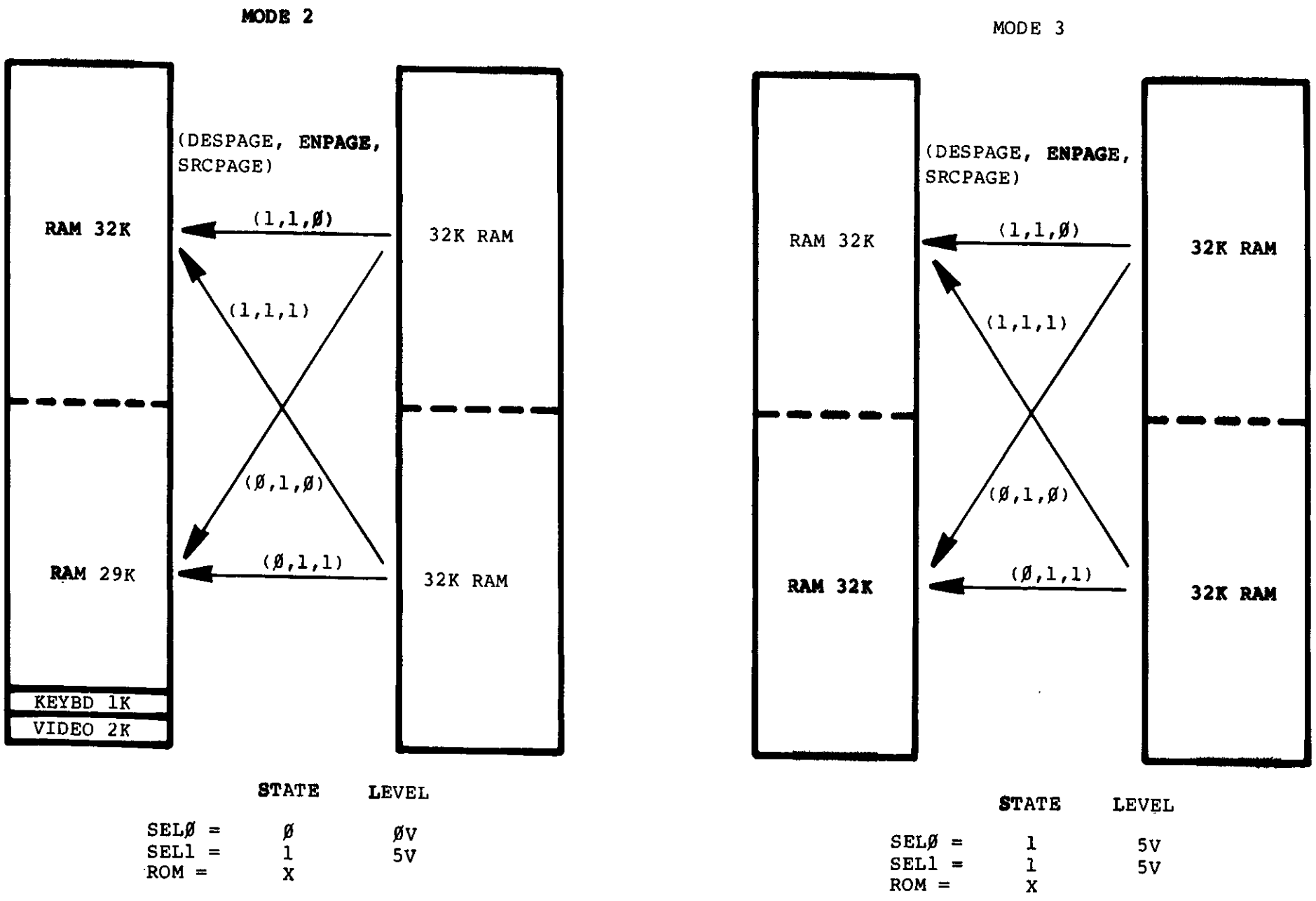


Figure 4-6. Memory

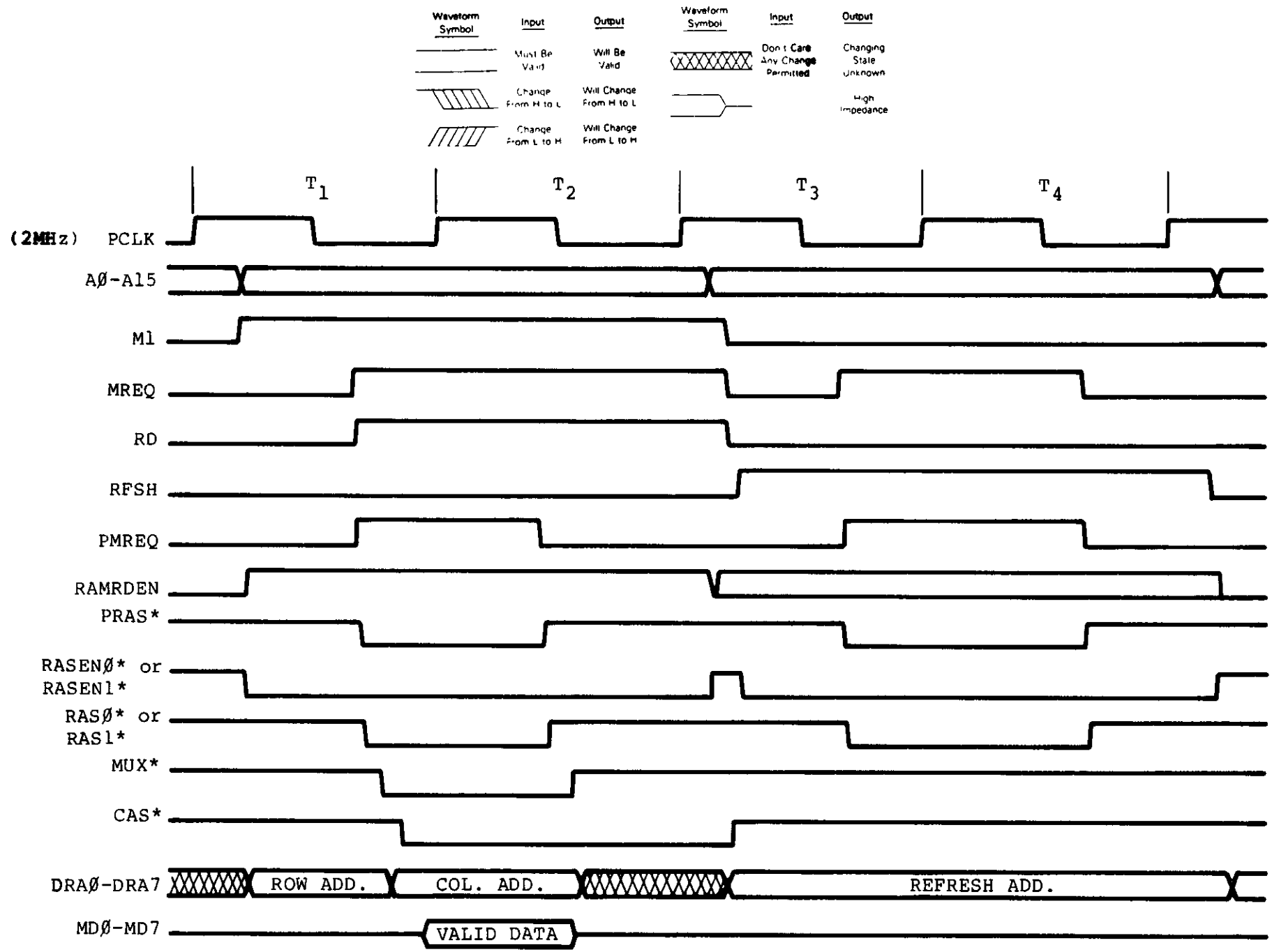


Figure 4-7. M[illegible]ycle Timing (2MHZ)

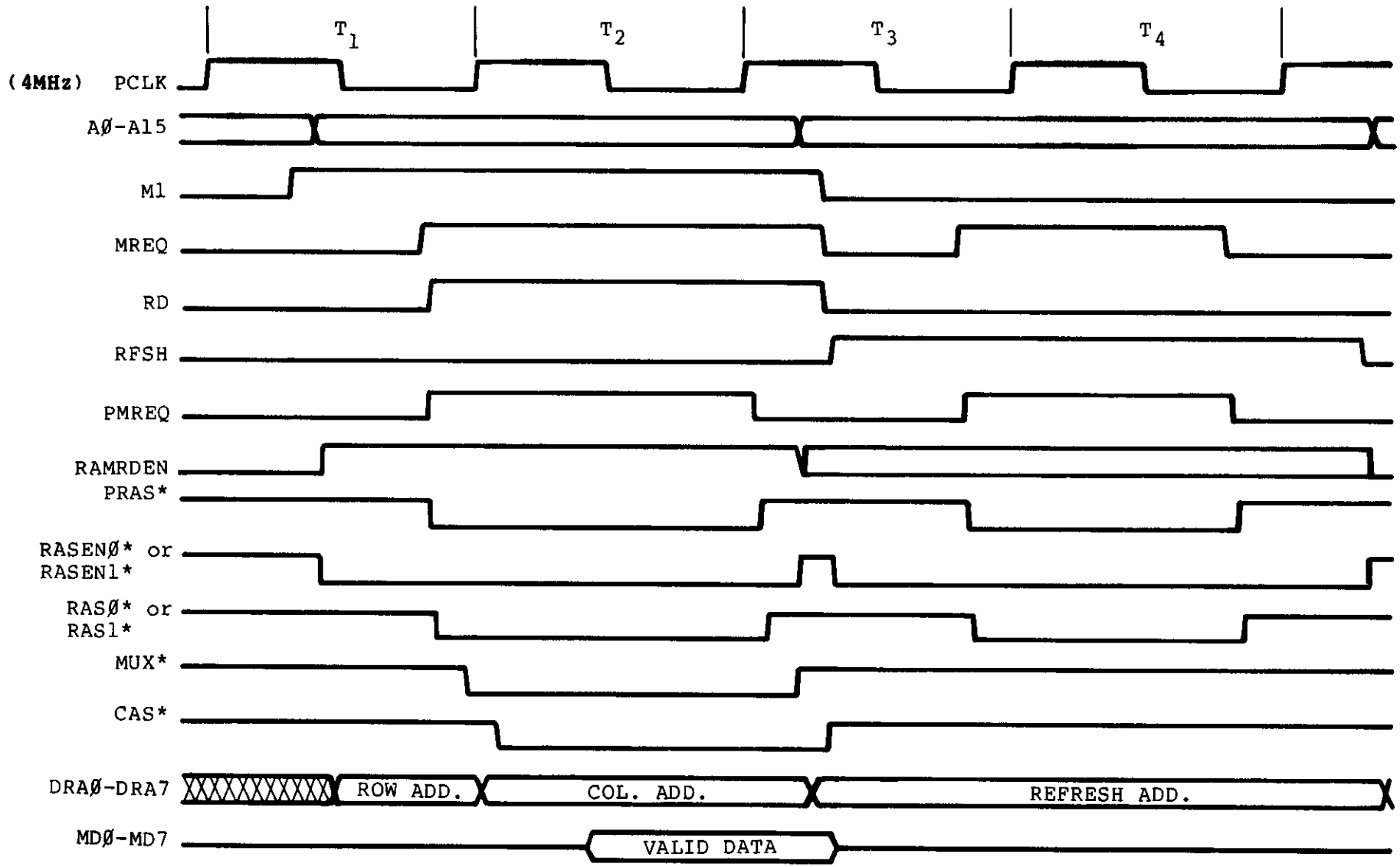


Figure 4-8. M1 Cycle Timing (4MHZ)

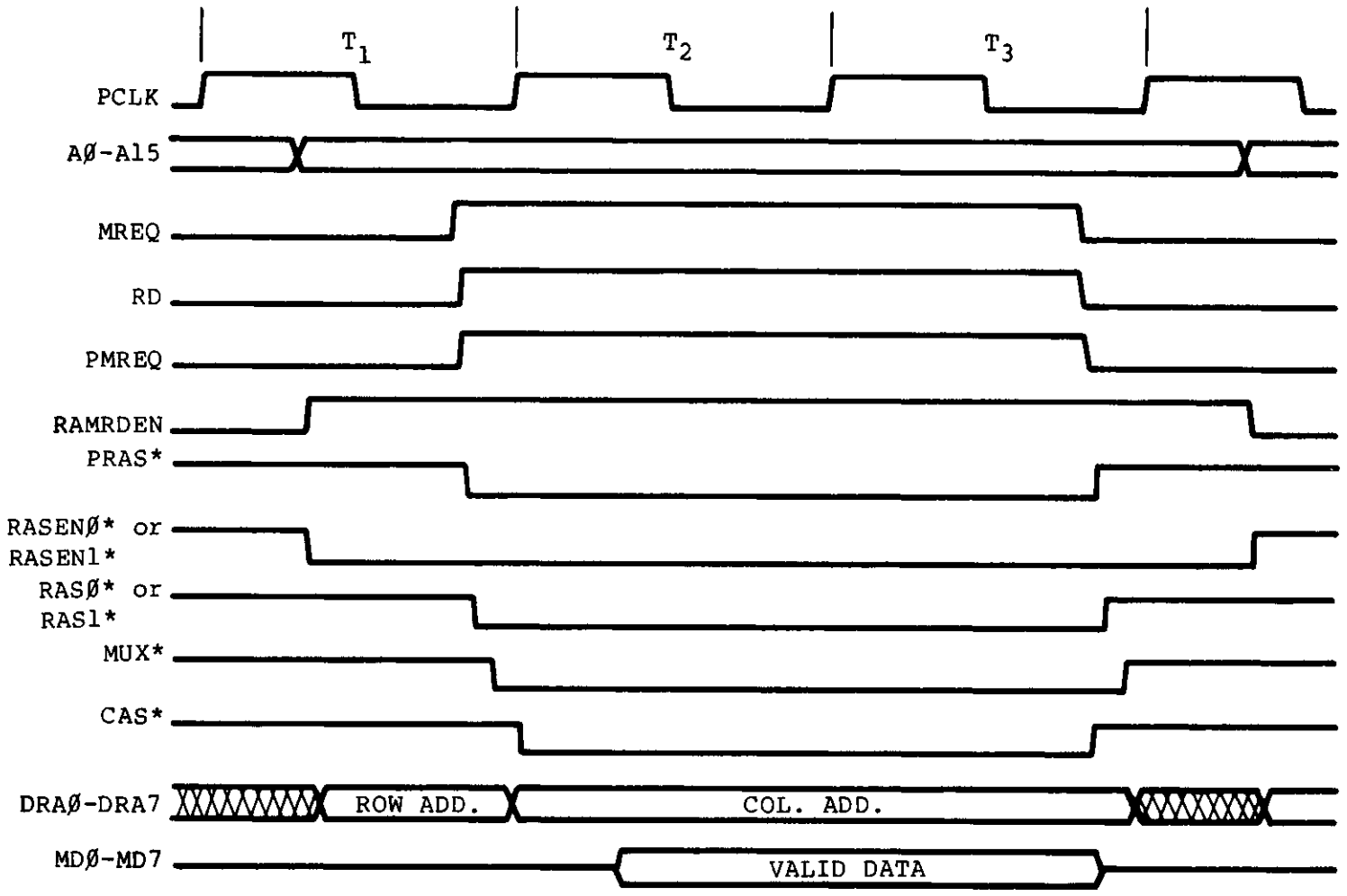


Figure 4-9. Memory Read Cycle Timing

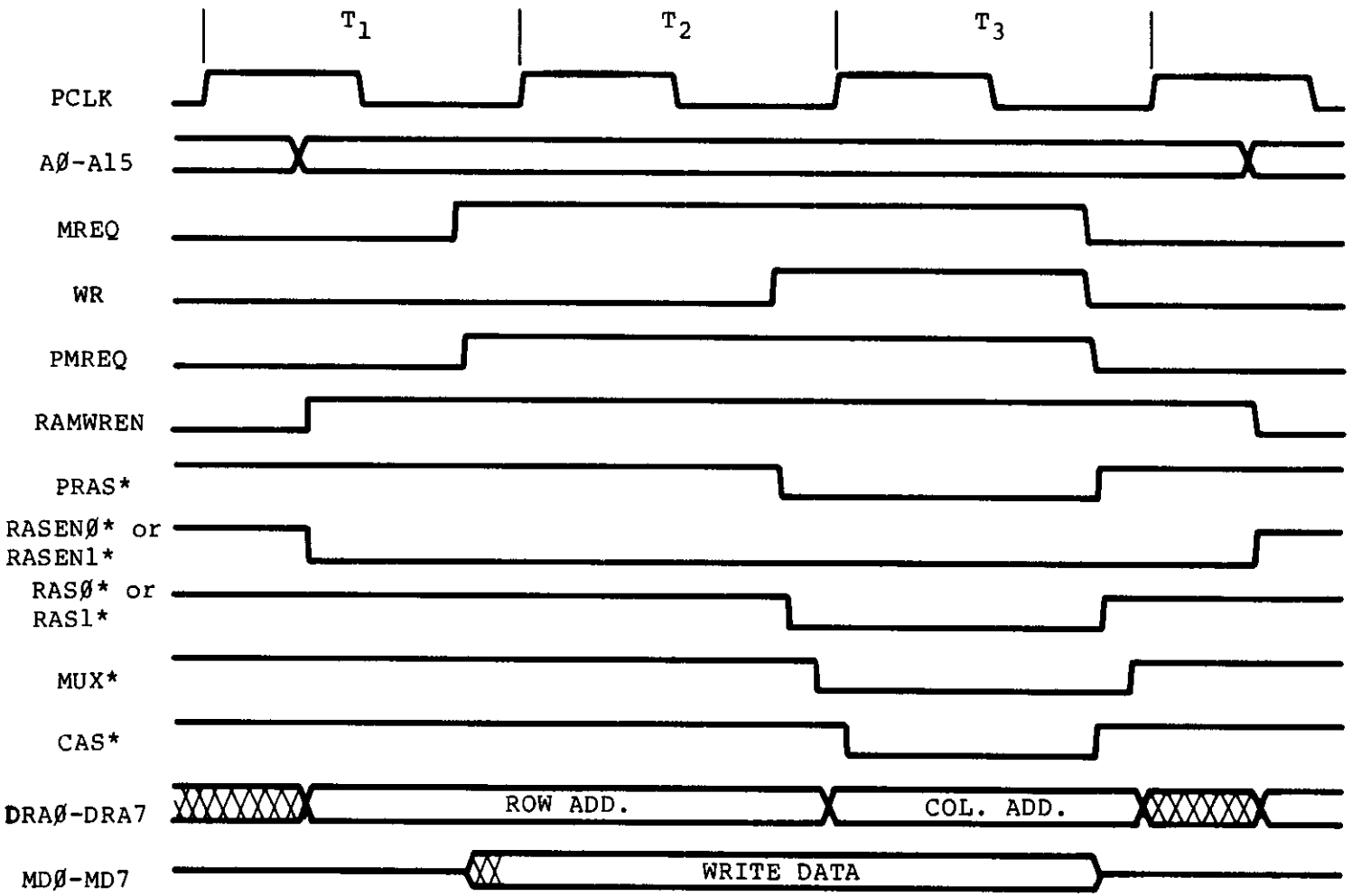


Figure 4-10. Memory Write Cycle Timing

Mode 0 — SEL0 = 0 = 0V; SEL1 = 0 = 0V; ROM = 1 = 0V

0000 — 0FFF	Boot ROM	4K
1000 — 37FF	RAM (Read Only)	10K
37E8 — 37E9	Printer Status (Read Only)	2
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 0 — SEL0 = 0 = 0V; SEL1 = 0 = 0V; ROM = 0 = +5V

0000 — 37FF	RAM (Read Only)	14K
37E8 — 37E9	Printer Status (Read Only)	2
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 1 — SEL0 = 1 = +5V; SEL1 = 0 = 0V; ROM = 1 = 0V

0000 — 0FFF	Boot ROM	4K
0000 — 0FFF	RAM (Write Only)	4K
1000 — 37FF	RAM	10K
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 1 — SEL0 = 1 = +5V; SEL1 = 0 = 0V; ROM = 0 = +5V

0000 — 37FF	RAM	14K
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 2 — SEL0 = 0 = 0V; SEL1 = 1 = +5V; ROM = X = Don t Care

0000 — F3FF	RAM	61K
F400 — F7FF	Keyboard	1K
F800 — FFFF	Video	2K

Mode 3 — SEL0 = 1 = +5V; SEL1 = 1 = +5V; ROM = X = Don t Care

0000 — FFFF	RAM	64K

I/O Port Assignment

Port #	Normally Used	Out	In
FC — FF	FF	CASSOUT *	MODIN *
F8 — FB	F8	LPOUT *	LPIN *
F4 — F7	F4	DRVSEL *	(RESERVED)
F0 — F3	–	DISKOUT *	DISKIN *
F0	F0	FDC COMMAND REG.	FDC STATUS REG.
F1	F1	FDC TRACK REG.	FDC TRACK REG.
F2	F2	FDC SECTOR REG.	FDC SECTOR REG.
F3	F3	FDC DATA REG.	FDC DATA REG.
EC — EF	EC	MODOUT *	RTCIN *
E8 — EB	–	RS232OUT *	RS232IN *
E8	E8	UART MASTER RESET	MODEM STATUS
E9	E9	BAUD RATE GEN. REG.	(RESERVED)
EA	EA	UART CONTROL AND MODEM CONTROL REG.	UART STATUS REG.
EB	EB	UART TRANSMIT HOLDING REG.	UART HOLDING REG. (RESET D.R.)
E4 — E7	E4	WR NMI MASK REG. *	RD NMI STATUS *
E0 — E3	E0	WR INT MASK REG. *	RD INT MASK REG. *
A0 — DF	–	(RESERVED)	(RESERVED)
9C — 9F	9C	BOOT *	(RESERVED)
94 — 9B	–	(RESERVED)	(RESERVED)
90 — 93	90	SEN *	(RESERVED)
8C — 8F	–	GSEL0 *	GSEL0 *
88 — 8B	–	CRTCCS *	(RESERVED)
88, 8A	88	CRCT ADD. REG.	(RESERVED)
89, 8B	89	CRCT DATA REG.	(RESERVED)
84 — 87	84	OPREG *	(RESERVED)
80 — 83	–	GSEL1 *	GSEL1 *

I/O Port Description

Name: CASSOUT *
Port Address: FC — FF
Access: WRITE ONLY
Description: Output data to cassette or for sound generation

Note: The Model 4P **does not** support cassette storage this port is only used to generate sound that was to be output via cassette port The Model 4P sends data to onboard sound circuit

D0 = Cassette output level (sound data output)

D1 = Reserved

D2 — D7 = Undefined

Name: MODIN * (CASSIN *)
Port Address: FC — FF
Access: READ ONLY
Description: Configuration Status

D0 = 0

D1 = CASSMOTORON STATUS

D2 = MODSEL STATUS

D3 = ENALTSET STATUS

D4 = ENEXTIO STATUS

D5 = (NOT USED)

D6 = FAST STATUS

D7 = 0

Name: LPOUT *
Port Address: F8 — FB
Access: WRITE ONLY
Description: Output data to line printer

D0 — D7 = ASCII BYTE TO BE PRINTED

Name: LPIN *
Port Address: F8 — FB
Access: READ ONLY
Description: Input line printer status

D0 — D3 = (RESERVED)

D4 = FAULT
1 = TRUE
0 = FALSE

D5 = UNIT SELECT
1 = TRUE
0 = FALSE

D6 = OUTPAPER
1 = TRUE
0 = FALSE

D7 = BUSY
1 = TRUE
0 = FALSE

Name: DRVSEL *
Port Address: F4 — F7
Access: WRITE ONLY
Description: Output FDC Configuration

Note: Output to this port will **ALWAYS** cause a 1-2 mscc (Microsecond) wait to the Z80

D0 = DRIVE SELECT 0

D1 = DRIVE SELECT 1

D2 = (RESERVED)

D3 = (RESERVED)

D4 = SDSEL
0 = SIDE 0
1 = SIDE 1

D5 = PRECOMPEN
0 = No write precompensation
1 = Write Precompensation enabled

D6 = WSGEN
0 = No wait state generated
1 = wait state generated

Note: This wait state is to sync Z80 with FDC chip during FDC operation

D7 = DDEN *
0 = Single Density enabled (FM)
1 = Double Density enabled (MFM)

Name: DISKOUT *
Port Address: F0 — F3
Access: WRITE ONLY
Description: Output to FDC Control Registers

Port F0 = FDC Command Register

Port F1 = FDC Track Register

Port F2 = FDC Sector Register

Port F3 = FDC Data Register

(Refer to FDC Manual for Bit Assignments)

Name: DISKIN *
Port Address: F0 — F3
Access: READ ONLY
Description: Input FDC Control Registers

Port F0 = FDC Status Register

Port F1 = FDC Track Register

Port F2 = FDC Sector Register

Port F3 = FDC Data Register

(Refer to FDC Manual for Bit Assignment)

Name: MODOUT *
Port Address: EC — EF
Access: WRITE ONLY
Description: Output to Configuration Latch

D0 = (RESERVED)

D1 = CASSMOTORON (Sound enable)
0 = Cassette Motor Off (Sound enabled)
1 = Cassette Motor On (Sound disabled)

D2 = MODSEL
0 = 64 or 80 character mode
1 = 32 or 40 character mode

D3 = ENALTSET
0 = Alternate character set disabled
1 = Alternate character set enabled

D4 = ENEXTIO
0 = External IO Bus disabled
1 = External IO Bus enabled

D5 = (RESERVED)

D6 = FAST
0 = 2 MHZ Mode
1 = 4 MHZ Mode

D7 = (RESERVED)

Name: RTCIN *
Port Address: EC — EF
Access: READ ONLY
Description: Clear Real Time Clock Interrupt

D0 — D7 = DON T CARE

Name: RS232OUT *
Port Address: E8 — EB
Access: WRITE ONLY
Description: UART Control, Data Control, Modem Control BRG Control

Port E8 = UART Master Reset

Port E9 = BAUD Rate Gen Register

Port EA = UART Control Register (Modem Control Reg)

Port EB = UART Transmit Holding Reg

(Refer to Model III or 4 Manual for Bit Assignments)

Name: RS232IN *
Port Address: E8 — EB
Access: READ ONLY
Description: Input UART and Modem Status

Port E8 = MODEM STATUS

Port E9 = (RESERVED)

Port EA = UART Status Register

Port EB = UART Receive Holding Register (Resets DR)

(Refer to Model III or 4 Manual for Bit Assignments)

Name: WRNMIMASKREG *
Port Address: E4 — E7
Access: WRITE ONLY
Description: Output NMI Latch

D0 — D5 (RESERVED)

D6 - ENMOTOROFFINT
0 Disables Motoroff NMI
1 - Enables Motoroff NMI

D7 - ENINTRQ
0 - Disables INTRQ NMI
1 - Enables INTRQ NMI

Name: RDNMISTATUS *
Port Address: E4 — E7
Access: READ ONLY
Description: Input NMI Status

D0 = 0

D2 — D4 - (RESERVED)

D5 = RESET (not needed)
0 - Reset Asserted (Problem)
1 - Reset Negated

D6 = MOTOROFF
0 - Motoroff Asserted
1 - Motoroff Negated

D7 = INTRQ
0 = INTRQ Asserted
1 = INTRQ Negated

Name: WRINTMASKREG *
Port Address: E0 — E3
Access: WRITE ONLY
Description: Output INT Latch

D0 — D1 = (RESERVED)

D2 = ENRTC
0 = Real time clock interrupt disabled
1 - Real time clock interrupt enabled

D3 = ENIOBUSINT
0 = External IO Bus interrupt disabled
1 = External IO Bus interrupt enabled

D4 = ENXMITINT
0 = RS232 Xmit Holding Reg empty int disabled
1 = RS232 Xmit Holding Reg empty int enabled

D5 = ENRECINT
0 RS232 Rec Data Reg full int disabled
1 - RS232 Rec Data Reg full int enabled

D6 - ENERRORINT
0 - RS232 UART Error interrupts disabled
1 - RS232 UART Error interrupts enabled

D7 - (RESERVED)

Name: RDINTSTATUS *
Port Address: E0 — E3
Access: READ ONLY
Description: Input INT Status

D0 — D1 - (RESERVED)

D2 - RTC INT

D3 = IOBUS INT

D4 = RS232 XMIT INT

D5 = RS232 REC INT

D6 = RS232 UART ERROR INT

D7 = (RESERVED)

Name: BOOT *
Port Address: 9C — 9F
Access: WRITE ONLY
Description: Enable or Disable Boot ROM

D0 = ROM *
0 - Boot ROM Disabled
1 = Boot ROM Enabled

D1 — D7 = (RESERVED)

Name: SEN *
Port Address: 90 — 93
Access: WRITE ONLY
Description: Sound output

D0 = SOUND DATA

D1 — D7 = (RESERVED)

Name: OPREG *
Port Address: 84
Access: WRITE ONLY
Description: Output to operation reg.

D0 = SEL0

D1 = SEL1

SEL1	SEL0	MODE
0	0	0
0	1	1
1	0	2
1	1	3

D2 = 8064
0 = 64 character mode
1 = 80 character mode

D3 = INVERSE
0 = Inverse video disabled
1 = Inverse video enabled

D4 = SRCPAGE — Points to the page to be mapped as new page
0 = U64K, L32K Page
1 = U64K, U32K Page

D5 = ENPAGE — Enables mapping of new page
0 = Page mapping disabled
1 = Page mapping enabled

D6 = DESPAGE — Points to the page where new page is to be mapped:
0 = L64K, U32K Page
1 = L64K, L32K Page

D7 = PAGE
0 = Page 0 of Video Memory
1 = Page 1 of Video Memory

4.2.8 Video Circuit

The heart of the video display circuit in the Model 4P is the 68045 Cathode Ray Tube Controller (CRTC) U42 The CRTC is a preprogrammed video controller that provides two screen formats 64 by 16 and 80 by 24 The format is controlled by pin 3 of the CRTC (8064*) The CRTC generates all of the necessary signals required for the video display These signals are VSYNC (Vertical Sync), HSYNC (Horizontal Sync) for proper sync of the monitor DISPEN (Display Enable) which indicates when video data should be output to the monitor, the refresh memory addresses (MA0-MA13) which addresses the video RAM, and the row addresses (RA0-RA4) which indicates which scan line row is being displayed The CRTC also provides hardware scrolling by writing to the internal Memory Start Address Register by OUTing to Port 88H The internal cursor control of the 68045 is not used in the Model 4P video circuit

Since the 80 by 24 screen requires 1,920 screen memory locations, a 2K by 8 static RAM (U82) is used for the video RAM Addressing to the video RAM (U82) is provided by the 68045 when refreshing the screen and by the CPU when updating of the data is performed These two sets of address lines are multiplexed by three 74LS157s (U41, U61, and U81) The multiplexers are switched by CRTCLK which allows the CRTC to address the video RAM during the high state of CRTCLK and the CPU access during the low state A10 from the CPU is controlled by PAGE* which allows two display pages in the 64 by 16 format When updates to the video RAM are performed by the CPU, the CPU is held in a WAIT state until the CRTC is not addressing the video RAM This operation allows reads and writes to video RAM without causing hashing on the screen The circuit that performs this function is a 74LS244 buffer (U84), an 8 bit transparent latch, 74LS373 (U83) and a Delay line circuit shared with Dynamic RAM timing circuit consisting of a 74LS74 (U98), 74LS32 (U96), 74LS04 (U95), 74LS00 (U92), 74LS02 (U69), and Delay Line (U94) During a CPU Read Access to the Video RAM, the address is decoded by the GA 4 2 and asserts VIDEO* low This is inverted by U95 (1 6 of 74LS04) which pulls one input of U92 (1 4 of 74LS00) and in turn asserts VWAIT * low to the CPU RD is high at this time and is latched into U98 (1 2 of 74LS74) on the rising edge of XADR7*, inverse of CRTCLK

When RD is latched by U98 the Q output goes low releasing WAIT* from the CPU The same signal also is sent to the Delay Line (U94) through U117 (1 4 of 74F08) The Delay line delays the falling edge 240 ns for VLATCH* which latches the read data from the video RAM at U83 The data is latched so the CRTC can refresh the next address location and prevent any hashing MRD* decoded by U106 and a memory read is ORed with VIDEO* which enables the data from U83 to the data bus The CPU then reads the data and completes the cycle A CPU write is slightly more complex in operation As in the RD cycle, VIDEO* is asserted low which asserts VWAIT* low to the CPU WR is high at this time which is NANDed with VIDEO and synced with CRTCLK to create VRAMDIS that disables the video RAM output On the rising edge of XADR7*, WR is latched into U98 (1 2 of 74LS74) which releases VWAIT* and starts cycle through the Delay Line After 30ns DLYVWR* (Delayed video write) is asserted low which also asserts VBUFEN* (Video Buffer Enable) low VBUFEN* enabled data from the Data bus to the video RAM Approximately 120ns later DLYVWR* is negated high which writes the data to the video RAM and negates VBUFEN* turning off buffer The CPU then completes WR cycle to the video RAM Refer to Video RAM CPU Access Timing Figure 5-12 for timing of above RD or WR cycles

During screen refresh, CRTCLK is high allowing the CRTC to address Video RAM The data out of the video RAM is latched by LOAD* into Gate Array 4 3 (U102) INVERSE* determines if character should be alpha-numeric only (INVERSE* high) or unchanged (INVERSE* low) A9 is decoded with ENALTSET (Enable Alternate Set) and 7, which controls the alternate set in the character generator ROM See ENALTSET Control Table below

ENALTSET	Q7	Q6	A9
0	0	0	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

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During screen refresh, CRTCLK is high allowing the CRTC to address Video RAM The data out of the video RAM is latched by LOAD* into Gate Array 4 3 (U102) INVERSE* determines if character should be alpha-numeric only (INVERSE* high) or unchanged (INVERSE* low) A9 is decoded with ENALTSET (Enable Alternate Set) and 7, which controls the alternate set in the character generator ROM See ENALTSET Control Table below

ENALTSET	Q7	Q6	A9
0	0	0	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

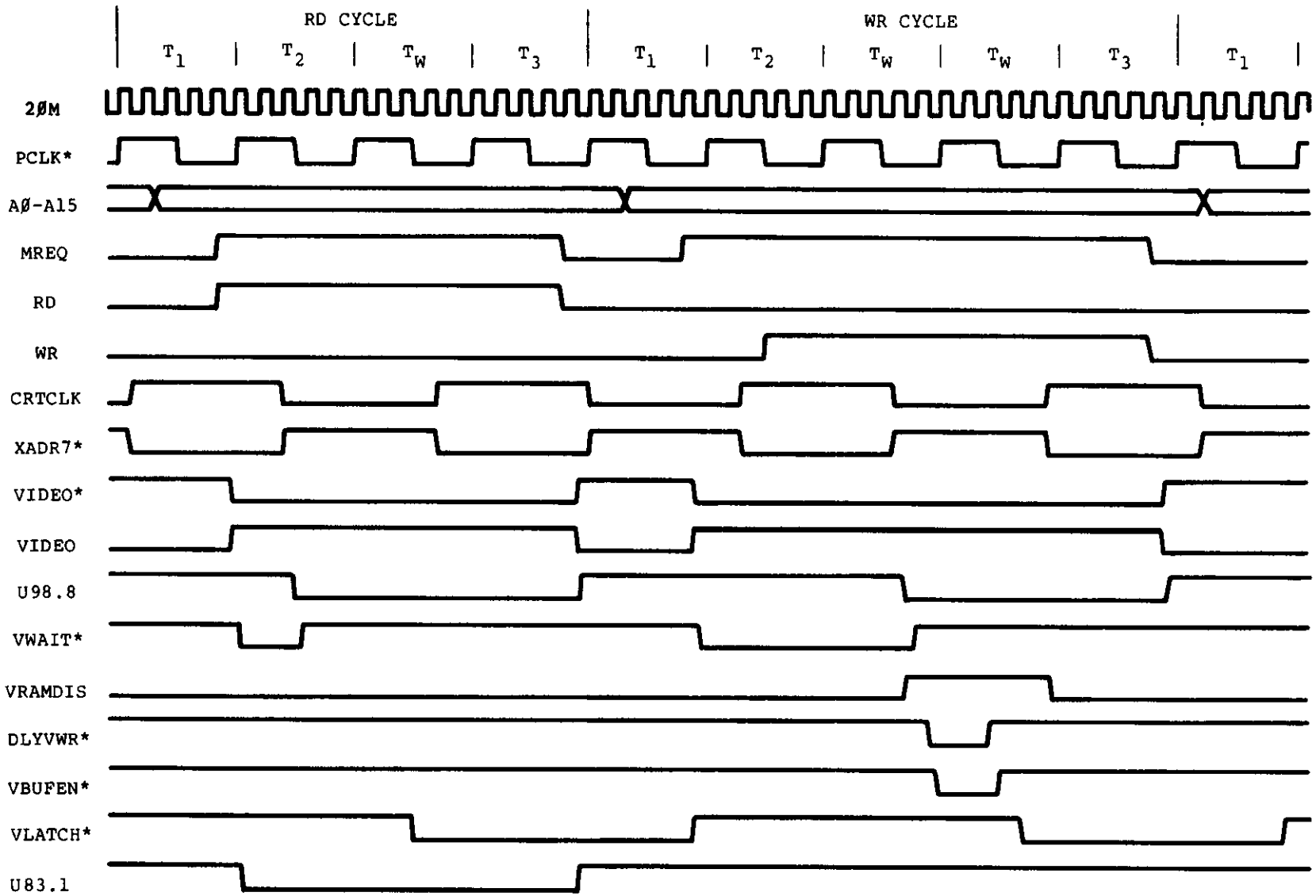


Figure 4-11. Video RAM CPU Access Timing

RA0-RA3, row addresses from the CRTC are used to control which scan line is being displayed The Model 4P has a 4-bit full adder 74LS283 (U101) to modify the Row address During a character display DLYGRAPHIC* is high which applies a high to all 4 bits to be added to row address This will result in subtract ing one from Row address count and allow all characters to be displayed one scan line lower The purpose is so inverse characters will appear within the inverse block When a graphic block is displayed DLYGRAPHIC* is low which causes the row address to be unmodified Moving jumper from E14-E15 to E15-E16 will disable this circuit

DLYCHAR* and DLYGRAPHICS are inverse signals and control which data is to be loaded into the internal shift register of U102 When DLYCHAR* is low and DLYGRAPHIC* is high, the Character Generator ROM (U103) is enabled to output data When DLYCHAR* is high and DLYGRAPHIC* is low the graphics characters are internally buffered to the shift register The data is loaded into the internal shift register on the rising edge of SHIFT* when LOADS* is low Serial video data is output U102 19 The video information is inverted by U142 and F83, is filtered by R14 (47 ohm resistor), and C227 (100 pf Cap) and output to video monitor VSYNC and HSYNC are buffered by (1/2 of 74LS86) U143 and are also output to video monitor Refer to Video Circuit Timing Figure 4-12 and Inverse Video Timing Figure 4-13 for timing relationships of Video Circuit

4.2.9 Keyboard

The keyboard interface of the Model 4P consists of open collector drivers which drive an 8 by 8 key matrix keyboard and an inverting buffer which buffers the key or keys pressed on the data bus The open collector drivers (U57 and U77 (7416) are driven by address lines A0-A7 which drive the column lines of the keyboard matrix The ROW lines of the keyboard are pulled up by a 1 5 kohm resistor pack RP2 The ROW lines are buffered and inverted onto the data bus by U78 (74LS240) which is enabled when KEYBD* is a logic low KEYBD* is a memory mapped decode of addresses 3800-3BFF in Model III Mode and F400-F7FF in Model 4/4P mode Refer to the Memory Map under Address Decode for more information During real time operation, the CPU will scan the keyboard periodically to check if any keys are pressed If no key is pressed, the resistor pack RP2 keeps the inputs of U78 at a logic high U78 inverts the data to a logic low and buffers it to the data bus which is read by the CPU If a key is pressed when the CPU scans the correct column line, the key pressed will pull the corresponding row to a logic low U78 inverts the signal to a logic high which is read by the CPU

4.2.10 Real Time Clock

The Real Time Clock circuit in the Model 4P provides a 30 Hz (in the 2 MHz CPU mode) or 60 Hz (in the 4 MHz CPU mode) interrupt to the CPU By counting the number of interrupts that have occurred the CPU can keep track of the time The 60 Hz vertical sync signal (VSYNC) from the video circuitry is used for the Real Time Clock s reference In the 2 MHz mode, FAST is a logic low which sets the Preset input pin 4 of U23 (74LS74) to a logic high This allows the 60 Hz (VSYNC) to be divided by 2 to 30 Hz The output of 1/2 of U23 is ORed with the original 60 Hz and then clocks another 74LS74 (1 2 of U23) If the real time clock is enabled (ENRTC at a logic high), the interrupt is latched and pulls the INT* line low to the CPU When the CPU recognizes the interrupt, the pulse is counted and the latch reset by pulling RTCIN* low In the 4 MHz mode, FAST is a logic high which keeps the first half of U23 in a preset state (the Q* output at a logic low) The 60 Hz is used to clock the interrupts

NOTE: If interrupts are disabled, the accuracy of the real time clock will suffer

4.2.11 Line Printer Port

The Line Printer Port Interface consists of a pulse generator, an eight-bit latch, and a status line buffer The status of the line printer is read by the CPU by enabling buffer U3 (74LS244) This buffer is enabled by LPRD* which is a memory map and port map decode In Model III mode, only the status can be read from memory location 37E8 or 37E9 The status can be read in all modes by an input from ports F8-FB For a listing of the bit status, refer to Port Map section

After the printer driver software determines that the printer is ready for printing (by reading the correct status) the characters to be printed are output to Port F8-FB U2, a 74LS374 eight-bit latch, latches the character byte and outputs to the line printer One-half of U1 (74LS123), a one-shot, is then triggered which generates an appropriate strobe signal to the printer which signifies a valid character is ready The output of the one-shot is buffered by 1/6th of the U51 (74LS04) to prevent noise from the printer cable from false-triggering the one-shot

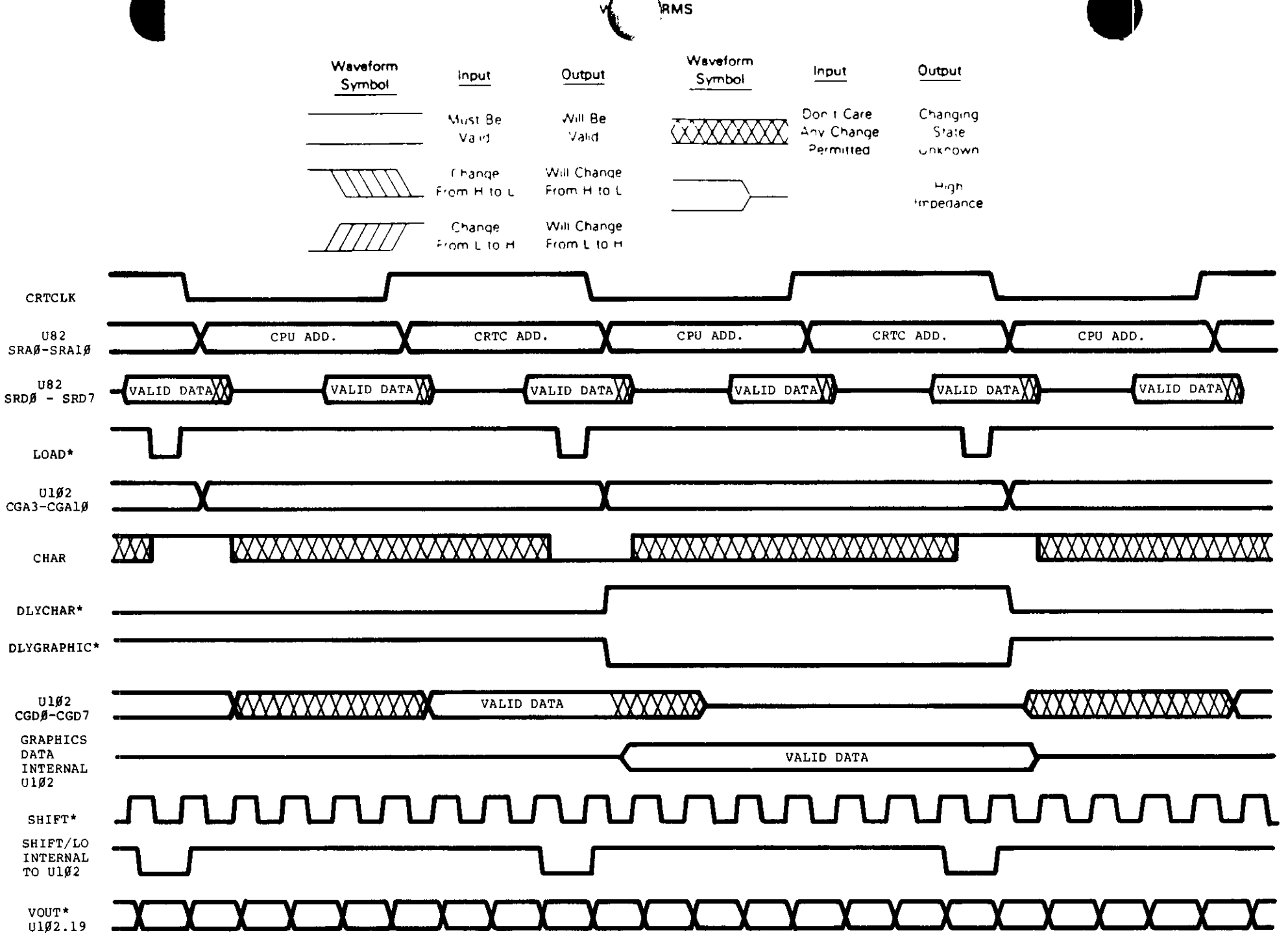


Figure 4-12. Video Circuit Timing

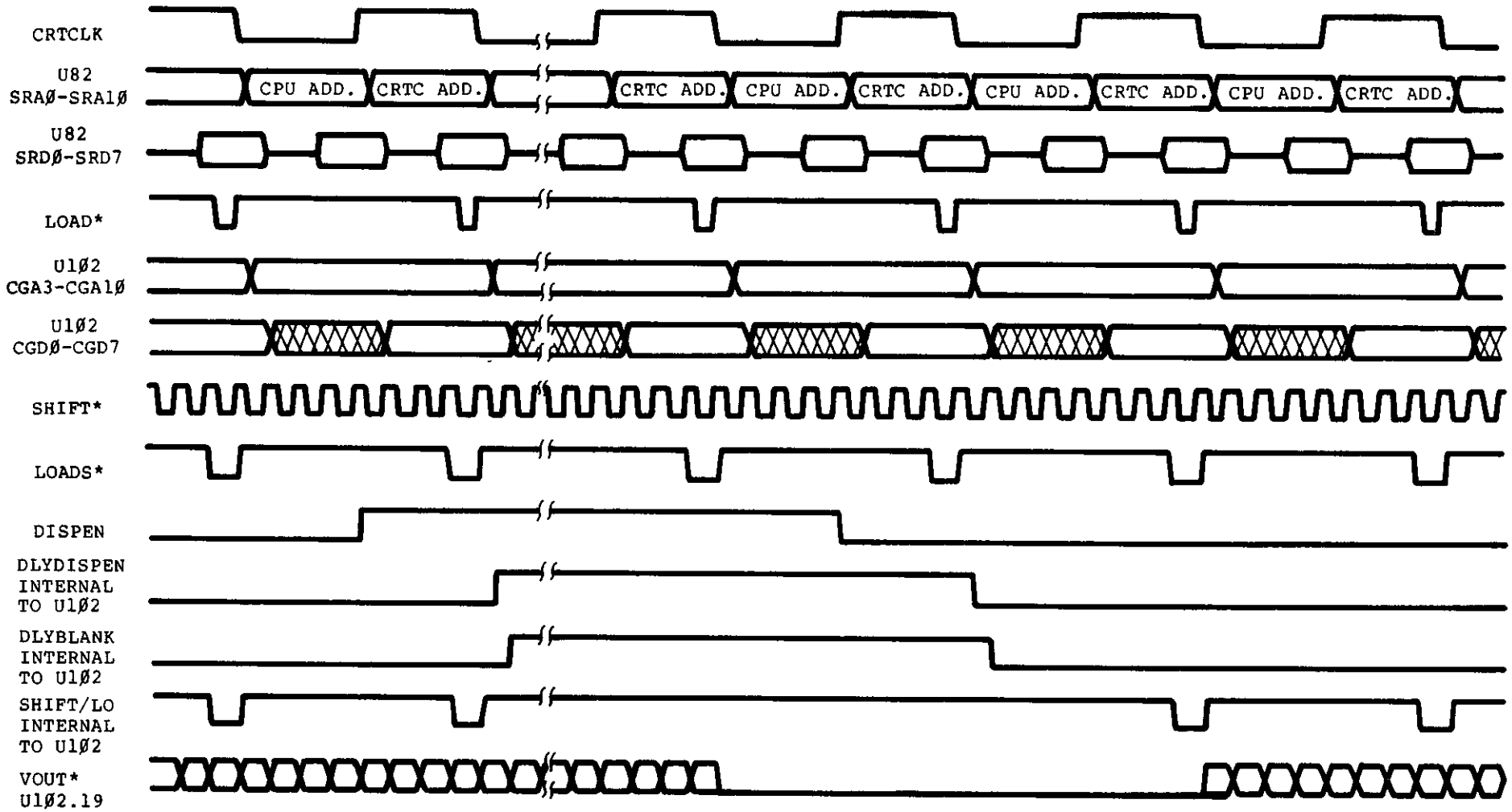


Figure 4-13. Video Blanking Timing

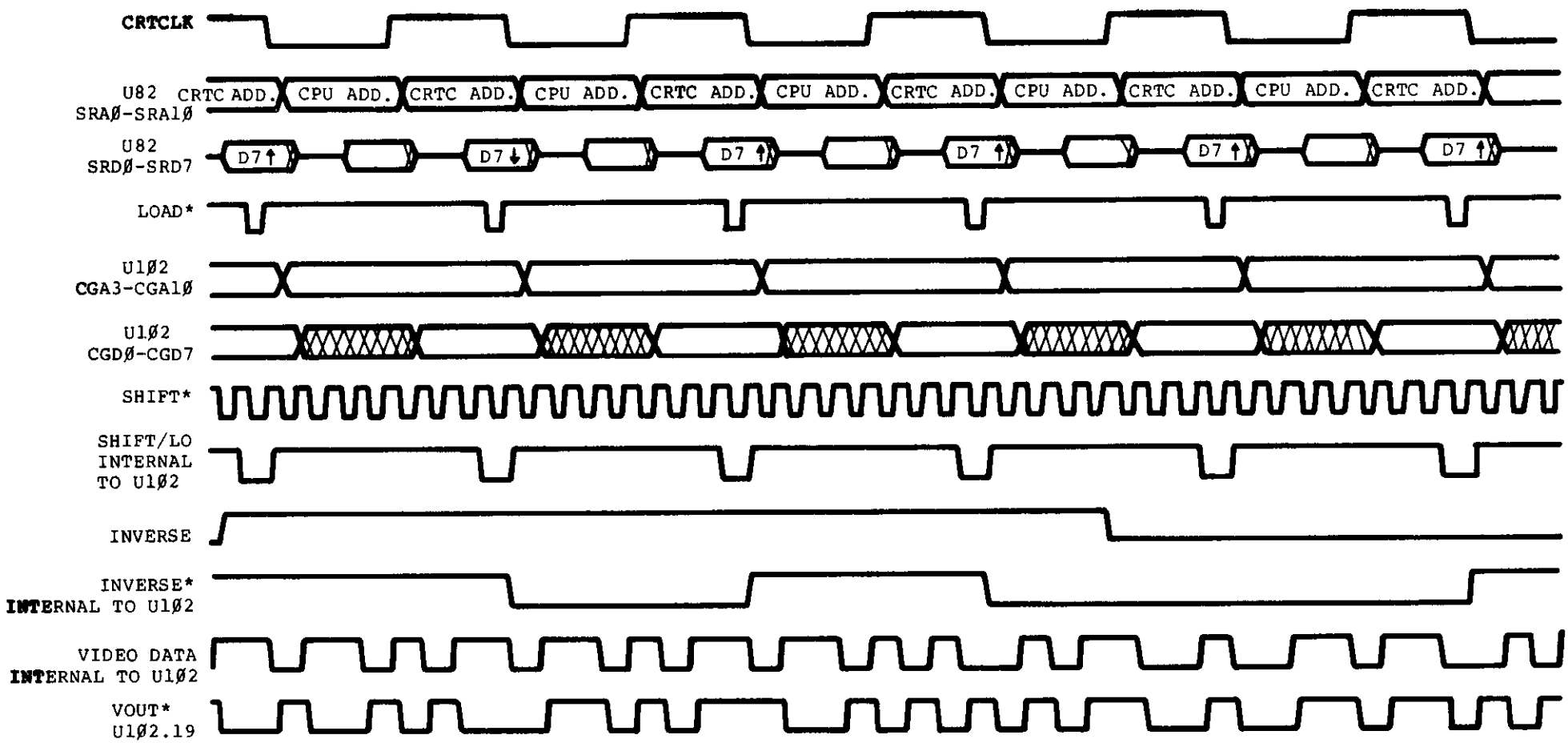


Figure 4-14. Inverse Video Timing

4.2.12 Graphics Port

The Graphics Port (J7) on the Model 4P is provided to attach the optional Graphics Board The port provides D0-D7 (Data Lines) A0-A3 (Address Lines) IN* GEN* and RESET* for the necessary interface signals for the Graphics Board GEN* is generated by negative ORing Port selects GSEL0* (8C-8FH) and GSEL1* (80-83H) together by (1 4 of 74LS08) U4 The resulting signal is negative ANDed with IORQ* by (1 4 of 74S32) U24 Seven timing signals are provided to allow synchronization of Main Logic Board Video and Graphics Board Video These timing signals are VSYNC, HSYNC, DISPEN, DCLK, H, I, and J Three control signals from the Graphics Board are used to sync to CPU access and select different video modes WAIT* controls the CPU access by causing the CPU to WAIT till video is in retrace area before allowing any writes or reads to Graphics Board RAM ENGRAF is asserted when Graphics video is displayed ENGRAF also disables inverse video mode on Main Logic Board Video CL166* (Clear 74L166) is used to enable or disable mixing of Main Logic Board Video and Graphics Board Video If CL166* is negated high, then mixing is allowed in all four video modes 80 x 24, 40 x 24, 64 x 16, and 32 x 16 If CL166* is asserted low, this will clear the video shift register U63, which allows no video from the Main Logic Board In this state 8064* is automatically asserted low to put screen in 80 x 24 video mode Refer to Figure 4-15 Graphic Board Video Timing for timing relationships Refer to the Model 4/4P Graphics Board Service information for service or technical information on the Graphics Board

4.2.13 Sound

The sound circuit in the Model 4P is compatible with the Sound Board which was optional in the Model 4 Sound is generated by alternately setting and clearing data bit D0 during an OUT to port 90H The state of D0 is latched by U129 (1 2 of a 74LS74) and the output is amplified by Q2 which drives a 8Ω speaker The speed of the software loop determines the frequency and thus, the pitch of the resulting tone Since the Model 4P does not have a cassette circuit, some existing software that used the cassette output for sound would have been lost The Model 4P routes the cassette latch to the sound board through U109 When the CASSMOTORON signal is a logic low the cassette motor is off, then the cassette output is sent to the sound circuit

4.2.14 I/O Bus Port

The Model 4P Bus is designed to allow easy and convenient interfacing of I O devices to the Model 4P The I O Bus supports all the signals necessary to implement a device compatible with the Z80s I O structure

Addresses

A0 to A7 allow selection of up to 256* input and 256 output devices if external I O is enabled

*Ports 80H to 0FFH are reserved for System use

Data

DB0 to DB7 allow transfer of 8-bit data onto the processor data bus is external I/O is enabled

Control Lines

1 M1* — Z80A signal specifying an M1 or Operation Code Fetch Cycle or with IOREQ* it specifies an Interrupt acknowledge

2 IN* — Z80A signal specifying than an input is in progress Logic AND of IOREQ* and WR*

3 OUT* — Z80A signal specifying that an output is in progress Logic AND of IOREQ* and WR*

4 IOREQ* — Z80A signal specifying that an input or output is in progress or with M1* it specifies an interrupt acknowledge

5 RESET* — system reset signal

6 IOBUSINT* — input to the CPU signaling an interrupt from an I O Bus device if I O Bus interrupts are enabled

7 IOBUSWAIT* — input to the CPU wait line allowing I O Bus device to force wait states on the Z80 if external I O is enabled

8 EXTIOSEL* — input to I O Bus Port circuit which switches the I O Bus data bus transceiver and allows and INPUT instruction to read I O Bus data

The address line data line and all control lines except RESET* are enabled only when the ENEXIO bit in port EC is set to one

To enable I O interrupts the ENIOBUSINT bit in the PORT E0 (output port) must be a one However even if it is disabled from generating interrupts the status of the IOBUSINT* line can still read on the appropriate bit of CPU IOPORT E0 (input port)

See Model 4P Port Bit assignments for port 0FF 0EC and 0E0

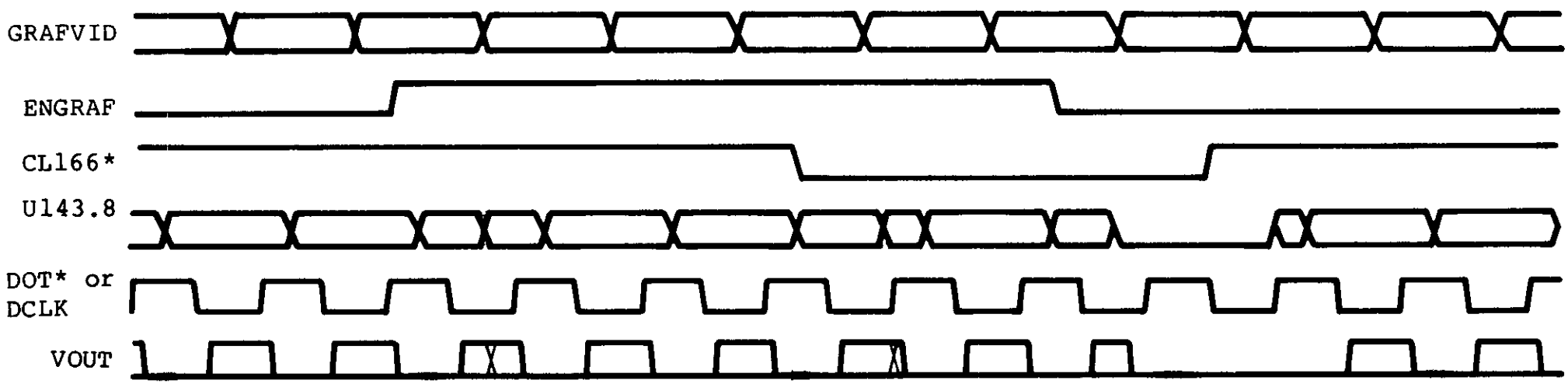


Figure 4-15. Graphic Board Video Timing

The Model 4P CPU board is fully protected from foreign I O devices in that all the I O Bus signals are buffered and can be disabled under software control To attach and use and I O device on the I O Bus certain requirements (both hardware and software) must be met

For input port device use, you must enable external I/O devices by writing to port 0ECH with bit 4 on in the user software This will enable the data bus address lines and control signals to the I/O Bus edge connector When the input device is selected, the hardware should acknowledge by asserting EXTIOSEL* low This switches the data bus transceiver and allows the CPU to read the contents of the I/O Bus data lines See Figure 4-16 for the timing EXTIOSEL* can be generated by NANDing IN and the I/O port address

Output port device use is the same as the input port device in use, in that the external I O devices must be enabled by writing to port 0ECH with bit 4 on in the user software — in the same fashion

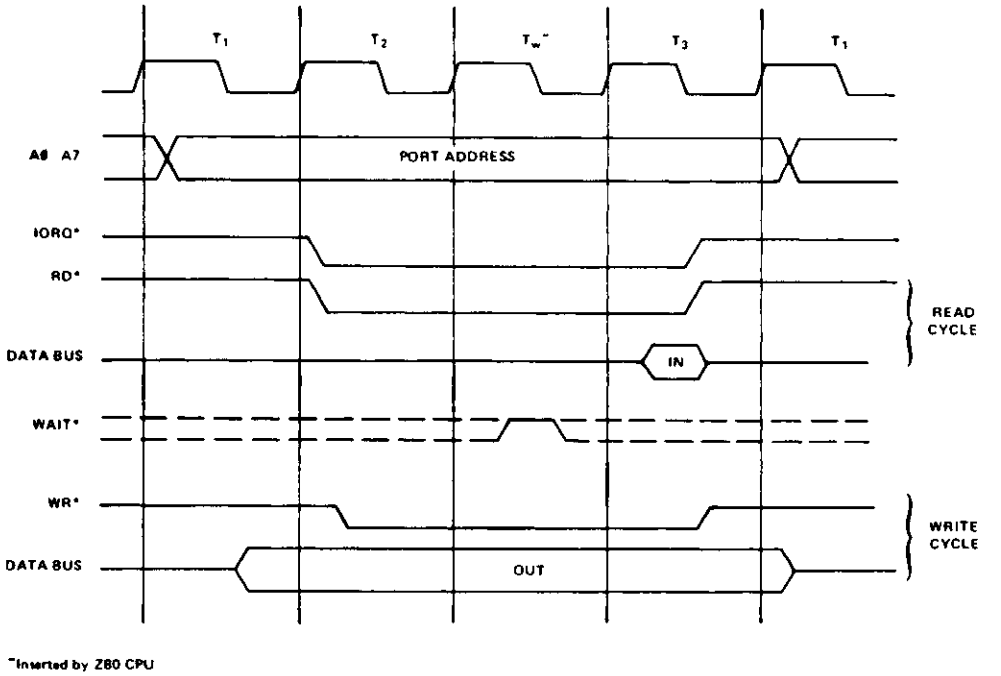
For either input or output devices, the IOBUSWAIT* control line can be used in the normal way for synchronizing slow devices to the CPU Note that since dynamic memories are used in the Model 4P, the wait line should be used with caution Holding the CPU in a wait state for 2 msec or more may cause loss of memory contents since refresh is inhibited during this time It is recommended that the IOBUSWAIT* line be held active no more than 500 µsec with a 25% duty cycle

The Model 4P will support Z80 Mode 1 interrupts A RAM jump table is supported by the LEVEL II BASIC ROMs image and the user must supply the address of his interrupt service routine by writing this address to locations 403E and 403F When an interrupt occurs, the program will be vectored to the user-supplied address if I/O Bus interrupts have been enabled To enable I/O Bus interrupts, the user must set bit 3 of Port 0E0H

4.2.15 FDC Circuit

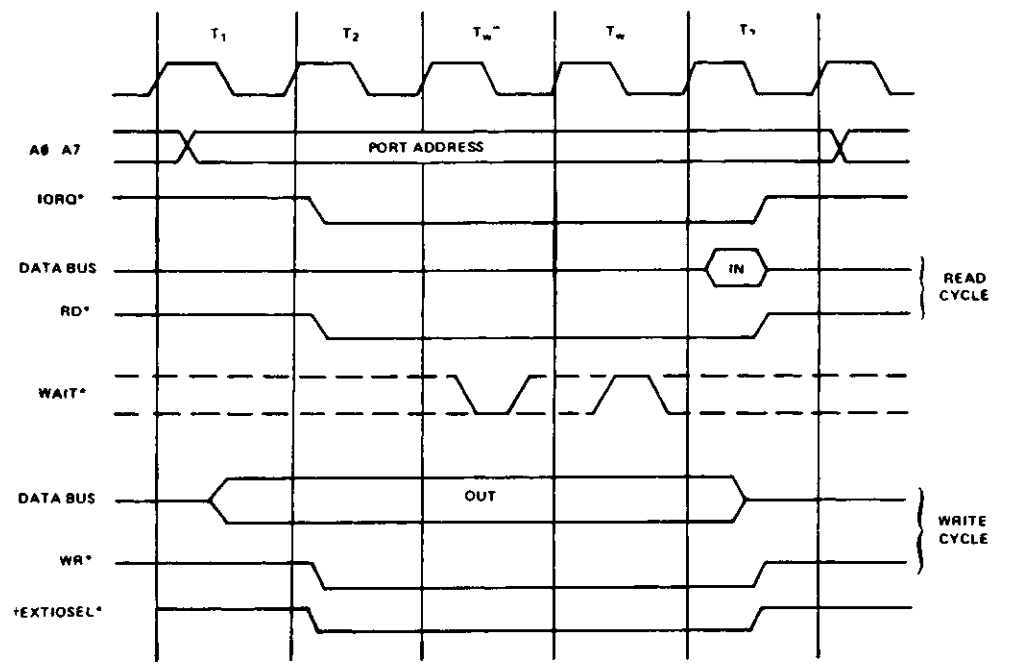
The TRS-80 Model 4P Floppy Disk Interface provices a standard 5-1 4 floppy disk controller The Floppy Disk Interface supports both single and double density encoding schemes Write precompensation can be software enabled or disabled beginning at any track, although the system software enables write precompensation for all tracks greater than twenty-one The amount of write precompensation is 125 nsec and is not adjustable One or two drives may be controlled by the interface All data transfers are accomplished by CPU data requests In double density operation, data transfers are synchronized to the CPU by forcing a wait to the CPU and clearing the wait by a data request from the FDC chip The end of the data transfer is indicated by generation of a non-maskable interrupt from the interrupt request output of the FDC chip A hardware watchdog timer insures that any error condition will not hang the wait line to the CPU for a period long enough to destroy RAM contents

Input or Output Cycles



*Inserted by Z80 CPU

Input or Output Cycles with Wait States



*Inserted by Z80 CPU

†Coincident with IORQ* only on INPUT cycle

Figure 4-16. I/O Bus Timing Diagram

Control and Data Buffering

The Floppy Disk Controller Board is an I O port mapped device which utilizes ports E4H F0H F1H F2H F3H and F4H The decoding logic is implemented on the CPU board (Refer to Paragraph 5 1 5 Address Decoding for more information on Port Map) U70 is a bi-directional 8-bit transceiver used to buffer data to and from the FDC and RS-232 circuits The direction of data transfer is controlled by the combination of control signals DISKIN* RS232IN* RDINT* and RDNMI* If any of these signals is active (logic low) U70 is enabled to drive data onto the CPU data bus If both signals are inactive (logic high) U70 is enabled to receive data from the CPU board data bus A second buffer (U36) is used to buffer the FDC chip data to the FDC RS232 Data Bus (BD0-BD7) U36 is enabled all the time and its direction controlled by DISKIN* Again if DISKIN* is active (logic low), data is enabled to drive from the FDC chip to the Main Data Busses If DISKIN* is inactive (logic high) data is enabled to be transferred to the FDC chip

Nonmaskable Interrupt Logic

Gate Array 4 4 (U18) is used to latch data bits D6 and D7 on the rising edge of the control signal WRNMI* This enables the conditions which will generate a non-maskable interrupt to the CPU The NMI interrupt conditions which are programmed by doing an OUT instruction to port E4H with the appropriate bits set If data bit 7 is set an FDC interrupt is enabled to generate an NMI interrupt If data bit 7 is reset interrupt requests request from the FDC are disabled If data bit 6 is set a Motor Time Out is enabled to generate an NMI interrupt If data bit 6 is reset, interrupts on Motor Time Out are disabled An IN instruction from port E4H enables the CPU to determine the source of the nonmaskable interrupt Data bit 7 indicates the status of FDC interrupt request (INTRQ) (0 = true, 1 = false) Data bit 6 indicates the status of Motor Time Out (0 = true, 1 = false) Data bit 5 indicates the status of the Reset signal (0 = true 1 = false) The control signal RDNMI* gates this status onto the CPU data bus when active (logic low)

Drive Select Latch and Motor ON Logic

Selecting a drive prior to disk I O operation is accomplished by doing an OUT instruction to port F4H with the proper bit set The following table describes the bit allocation of the Drive Select Latch

Data Bit	Function
D0	Selects Drive 0 when set*
D1	Selects Drive 1 when set*
D2	Selects Drive 2 when set*
D3	Selects Drive 3 when set*
D4	Selects Side 0 when reset Selects Side 1 when set
D5	Write precompensation enabled when set, disabled when reset
D6	Generates WAIT if set
D7	Selects MFM mode if set Selects FM mode if reset

*Only one of these bits should be set per output

Hex D flip-flop U54 (74L174) latches the drive select bits side select and FM* MFM bits on the rising edge of the control signal DRVSEL* Gate Array 4 4 (U18) is used to latch the Wait Enable and Write precompensation enable bits on the rising edge of DRVSEL* The rising edge of DRVSEL* also triggers a one-shot (1 2 of U54 74LS123) which produces a Motor On to the disk drives The duration of the Motor On signal is approximately three seconds The spindle motors are not designed for continuous operation Therefore the inactive state of the Motor On signal is used to clear the Drive Select Latch which de-selects any drives which were previously selected The Motor On one-shot is retriggerable by simply executing another OUT instruction to the Drive Select Latch

Wait State Generation and WAITIMOUT Logic

As previously mentioned, a wait state to the CPU can be initiated by an OUT to the Drive Select Latch with D6 set Pin 18 of U18 will go high after this operation This signal is inverted by 1/4th of U15 and is routed to the CPU where it forces the Z80A into a wait state The Z80A will remain in the wait state as long as WAIT* is low Once initiated, the WAIT* will remain low until one of five conditions is satisfied If INTRQ, DRQ and RESET, inputs become active (logic high) it causes WAIT* to go high which allows the Z80 to exit the wait state An internal timer in U18 serves as a watchdog timer to insure that a wait condition will not persist long enough to destroy dynamic RAM contents This internal watchdog timer logic will limit the duration of a wait to 1024μsec, even if the FDC chip should fail to generate a DRQ or an INTRQ

If an OUT to Drive Select Latch is initiated with D6 reset (logic low), a WAIT is still generated The internal timer in U18 will count to 2 which will clear the WAIT state This allows the WAIT to occur only during the OUT instruction to prevent violating any Dynamic RAM parameters

NOTE: This automatic WAIT will cause a 5-1 μsec wait each time an out to Drive Select Latch is performed

Clock Generation Logic

A 16 MHz crystal oscillator and a Gate Array 4.4 (U18) are used to generate the clock signals required by the FDC board. The 6 MHz oscillator is implemented internal to U18 and a quartz crystal (Y2). The output of the oscillator is divided by 2 to generate an 8 MHz clock. This is used by the FDC 1773 for all internal timing and data separation. U18 further divides the 16 MHz clock to drive the watchdog timer circuit.

Disk Bus Output Drivers

High current open collector drivers U15 and U34 are used to buffer the output signals from the FDC circuit to the disk drives.

Write Precompensation and Write Data Pulse Shaping Logic

All Write Precompensation is generated internal to the FDC chip 1773 (U17). Write Precompensation is enabled when W6 goes high and Write Precompensation is enabled from software. This signal is multiplexed with RDY by W6 is fed into pin 20 of U17. Write Data is output pin 22 of U17 and is shaped by a one-shot (1/2 of U56) which stretches the data pulses to approximately 500 nsec.

Floppy Disk Controller Chip

The 1773 is an MOS LSI device which performs the functions of a floppy disk formatter controller in a single chip implementation The following port addresses are assigned to the internal registers of the 1773 FDC chip

Port No.	Function
F0H	Command Status Register
F1H	Track Register
F2H	Sector Register
F3H	Data Register

4.2.16 RS-232-C Circuit

RS-232C Technical Description

The RS-232C circuit for the Model 4P computer supports asynchronous serial transmissions and conforms to the EIA RS-232C standards at the input-output interface connector (J4) The heart of the circuit is the TR1865 Asynchronous Receiver/Transmitter U33 It performs the job of converting the parallel byte data from the CPU to a serial data stream including start, stop, and parity bits For a more detailed description of how this LSI circuit performs these functions, refer to the TR1865 data sheets and application notes The transmit and receive clock rates that the TR1865 needs are supplied by the Baud Rate Generator U73 (BR1943) This circuit takes the 5 0688 MHz supplied by the system timing circuit and the programmed information received from the CPU over the data bus and divides the basic clock rate to provide two clocks The rates available from the BRG go from 50 Baud to 19200 Baud See the BRG table for the complete list

BRG Programming Table

Nibble Loaded	Transmit/ Receive Baud Rate	16X Clock	Supported by SETCOM
0H	50	0 8 kHz	Yes
1H	75	1 2 kHz	Yes
2H	110	1 76 kHz	Yes
3H	134 5	2 1523 kHz	Yes
4H	150	2 4 kHz	Yes
5H	300	4 8 kHz	Yes
6H	600	9 6 kHz	Yes
7H	1200	19 2 kHz	Yes
8H	1800	28 8 kHz	Yes
9H	2000	32 081 kHz	Yes
AH	2400	38 4 kHz	Yes
BH	3600	57 6 kHz	Yes
CH	4800	76 8 kHz	Yes
DH	7200	115 2 kHz	Yes
EH	9600	153 6 kHz	Yes
FH	19200	307 2 kHz	Yes

The RS-232C circuit is port mapped and the ports used are E8 to EB Following is a description of each port on both input and output

Port	Input	Output
E8	Modem status	Master Reset, enables UART control register load
EA	UART status	UART control register load and modem control
E9	Not Used	Baud rate register load enable bit
EB	Receiver Holding register	Transmitter Holding register

Interrupts are supported in the RS-232C circuit by the Interrupt mask register and the Status register internal to GA 4 5 (U31) which allow the CPU to see which kind of interrupt has occurred Interrupts can be generated on receiver data register full, transmitter register empty, and any one of the errors — parity, framing, or data overrun This allows a minimum of CPU overhead in transferring data to or from the UART The interrupt mask register is port E0 (write) and the interrupt status register is port E0 (read) Refer to the IO Port description for a full breakdown of all interrupts and their bit positions

All Model I, III, and 4 software written for the RS-232-C interface is compatible with the Model 4P RS-232-C circuit, provided the software does not use the sense switches to configure the interface. The programmer can get around this problem by directly programming the BRG and UART for the desired configuration or by using the SETCOM command of the disk operating system to configure the interface. The TRS-80 RS-232C Interface hardware manual has a good discussion of the RS-232C standard and specific programming examples (Catalog Number 26-1145).

Pinout Listing

The following list is a pinout description of the DB-25 connector (P1).

Pin No.	Signal
1	PGND (Protective Ground)
2	TD (Transmit Data)
3	RD (Receive Data)
4	RTS (Request to Send)
5	CTS (Clear To Send)
6	DSR (Data Set Ready)
7	SGND (Signal Ground)
8	CD (Carrier Detect)
19	SRTS (Spare Request to Send)
20	DTR (Data Terminal Ready)
22	RI (Ring Indicate)

Model 4P Gate Array
I/O Pin Assignments

J1		J2		J3	
Pin No.	**Signal**	**Pin No.**	**Signal**	**Pin No.**	**Signal**
1.	DATA STROBE	1.	XD0	1.	XD0
2.	GND	2.	GND	2.	GND
3.	PD0	3.	XD1	3.	XD1
4.	GND	4.	GND	4.	GND
5.	PD1	5.	XD2	5.	XD2
6.	GND	6.	GND	6.	GND
7.	PD2	7.	XD3	7.	XD3
8.	GND	8.	GND	8.	GND
9.	PD3	9.	XD4	9.	XD4
10.	GND	10.	GND	10.	GND
11.	PD4	11.	XD5	11.	XD5
12.	GND	12.	GND	12.	GND
13.	PD5	13.	XD6	13.	XD6
14.	GND	14.	GND	14.	GND
15.	PD6	15.	XD7	15.	XD7
16.	GND	16.	GND	16.	GND
17.	PD7	17.	XA0	17.	XA0
18.	GND	18.	GND	18.	GND
19.	N/A	19.	XA1	19.	XA1
20.	GND	20.	GND	20.	GND
21.	BUSY	21.	XA2	21.	XA2
22.	GND	22.	GND	22.	GND
23.	OUTPAPER	23.	XA3	23.	XA3
24.	GND	24.	GND	24.	GND
25.	UNIT SELECT	25.	XA4	25.	XA4
26.	NC	26.	GND	26.	GND
27.	GND	27.	XA5	27.	XA5
28.	FAULT	28.	GND	28.	GND
29.	N/A	29.	XA6	29.	XA6
30.	N/A	30.	GND	30.	GND
31.	NC	31.	XA7	31.	XA7
32.	N/A	32.	GND	32.	GND
33.	NC	33.	XIN*	33.	XIN*
34.	GND	34.	GND	34.	GND
35.		35.	XOUT*	35.	XOUT*
36.		36.	GND	36.	GND
37.		37.	XRESET*	37.	XRESET*
38.		38.	GND	38.	GND
39.		39.	IOBUSINT*	39.	IOBUSINT*
40.		40.	GND	40.	GND
41.		41.	IOBUSWAIT*	41.	IOBUSWAIT*
42.		42.	GND	42.	GND
43.		43.	EXTIOSEL*	43.	EXTIOSEL*
44.		44.	GND	44.	GND
45.		45.	NC	45.	NC
46.		46.	GND	46.	GND
47.		47.	XMI*	47.	XMI*
48.		48.	GND	48.	GND
49.		49.	XIOREQ*	49.	XIOREQ*
50.		50.	GND	50.	GND

J4

Pin No.	Signal
1.	PGND
2.	TD
3.	RD
4.	CTS
5.	DSR
6.	CD
7.	SGND
8.	CD
9.	
10.	
11.	
12.	
13.	
14.	
15.	
16.	
17.	
18.	
19.	SRTS
20.	DTR
21.	
22.	RI
23.	
24.	
25.	
26.	
27.	
28.	
29.	
30.	
31.	
32.	
33.	
34.	

J5

Pin No.	Signal
1.	GND
2.	
3.	GND
4.	
5.	GND
6.	
7.	GND
8.	DIP*
9.	GND
10.	DS0*
11.	GND
12.	DS1*
13.	GND
14.	
15.	GND
16.	MOTORON*
17.	GND
18.	DIR*
19.	GND
20.	STEP*
21.	GND
22.	WD*
23.	GND
24.	WG*
25.	GND
26.	DTRK0*
27.	GND
28.	DWPRT*
29.	GND
30.	DRRD*
31.	GND
32.	SDSEL
33.	GND
34.	

J7

Pin No.	Signal
1.	D0
2.	D1
3.	D2
4.	D3
5.	D4
6.	D5
7.	D6
8.	D7
9.	GEN*
10.	DCLK
11.	A0
12.	A1
13.	A2
14.	J
15.	GRAFVID
16.	ENGRAF
17.	DISPEN
18.	VSYNC
19.	HSYNC
20.	RESET*
21.	WAIT*
22.	H
23.	I
24.	IN*
25.	GND
26.	+5V
27.	
28.	CL166*
29.	GND
30.	+5V
31.	GND
32.	+5V
33.	GND
34.	+5V

J9

Pin No.	Signal
1.	GND
2.	VOUT
3.	GND
4.	VERTSYNC*
5.	GND
6.	HORZSYNC
7.	
8.	
9.	
10.	
11.	
12.	
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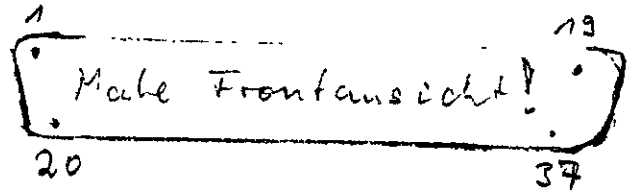
31.	
32.	
33.	
34.	

Herausgeführt auf externen Sub-D-Stecker 37pol.



1 ≙ 1
3 ≙ 2
5 ≙ 3 usw.

2 ≙ 20
4 ≙ 21
6 ≙ 22 usw.

SECTION V

CHIP SPECIFICATIONS

CHIP SPECIFICATIONS

4	4P	4 GATE ARRAY	4P GATE ARRAY
Motorola	**Motorola**	**Motorola**	**Motorola**
MC 6835	MC 6835	MC 6835	MC 6835
	Western Digital	**Western Digital**	**Western Digital**
	BR 1943	BR 1943	BR 1943
	(BR 1941L)		
	FD 1793	TR 1865	TR 1865
	(WD 179X)		
	FDC 9216	WD 1773	WD 1773
	TR 1865		
	WD 1943-00	**MATRA**	**MATRA**
MMI	**MMI**	Timing A. (4.1.1)	Timing A. (4.1.1)
PAL 16RGA (166)	PAL 16RGA S.T.	Address A. (4.2.0)	Address A. (4.2.0)
PAL 10L8 (208)	PAL 10L8 V.T.	Video A. (4.3.0)	Video A. (4.3.0)
	PAL 10L8 C.T.		
PAL 16L8 (268)	PAL 16L8 MeMep	**VTI**	**VTI**
PAL 16L8 (368)	PAL 16L8 Page Mep	FDC A. (4.4.0)	FDC A. (4.4.0)
		RS-232 A. (4.5.0)	RS-232 A. (4.5.0)
Zilog	**Zilog**	**Zilog**	**Zilog**
280 A	280 A	280 A	280 A

ARRAY #: 4.1.1

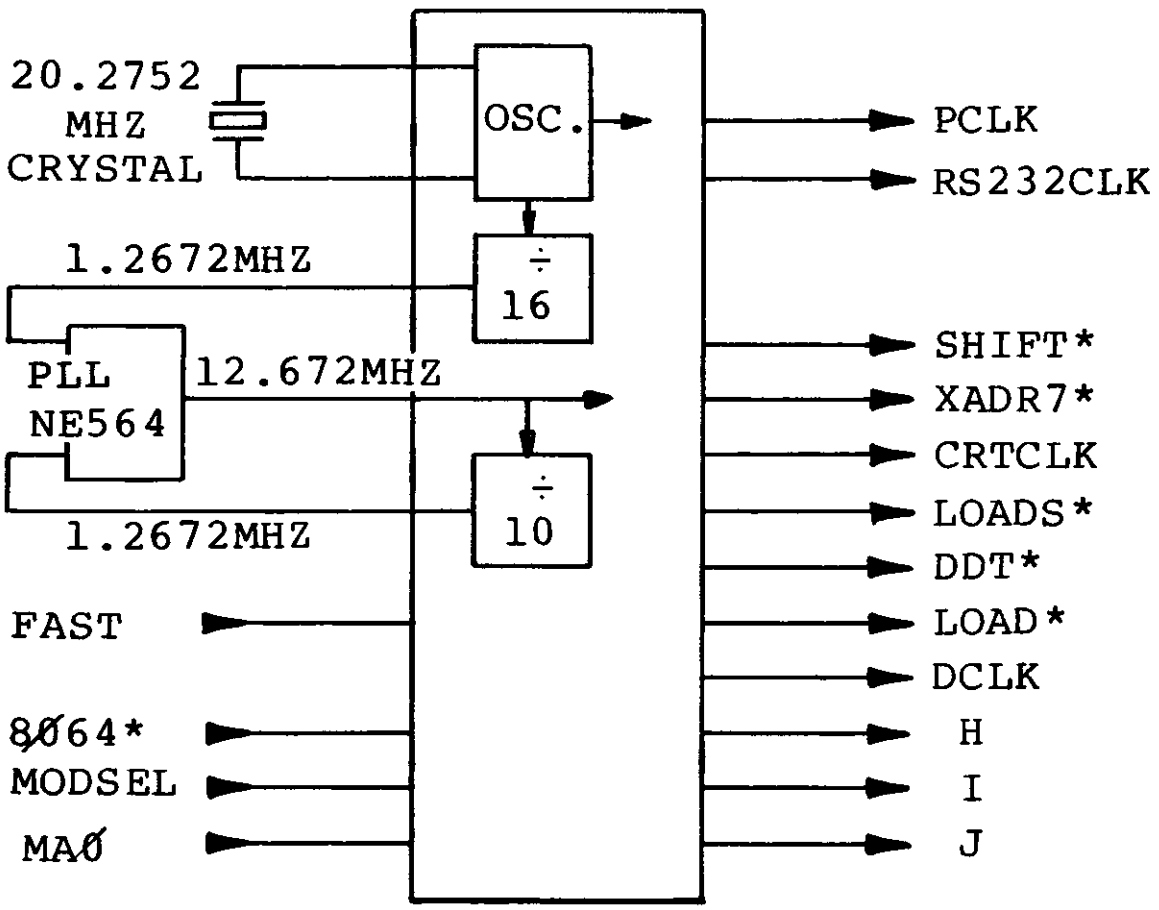
CIRCUIT NAME: System Timing

NO. OF PINS: 24

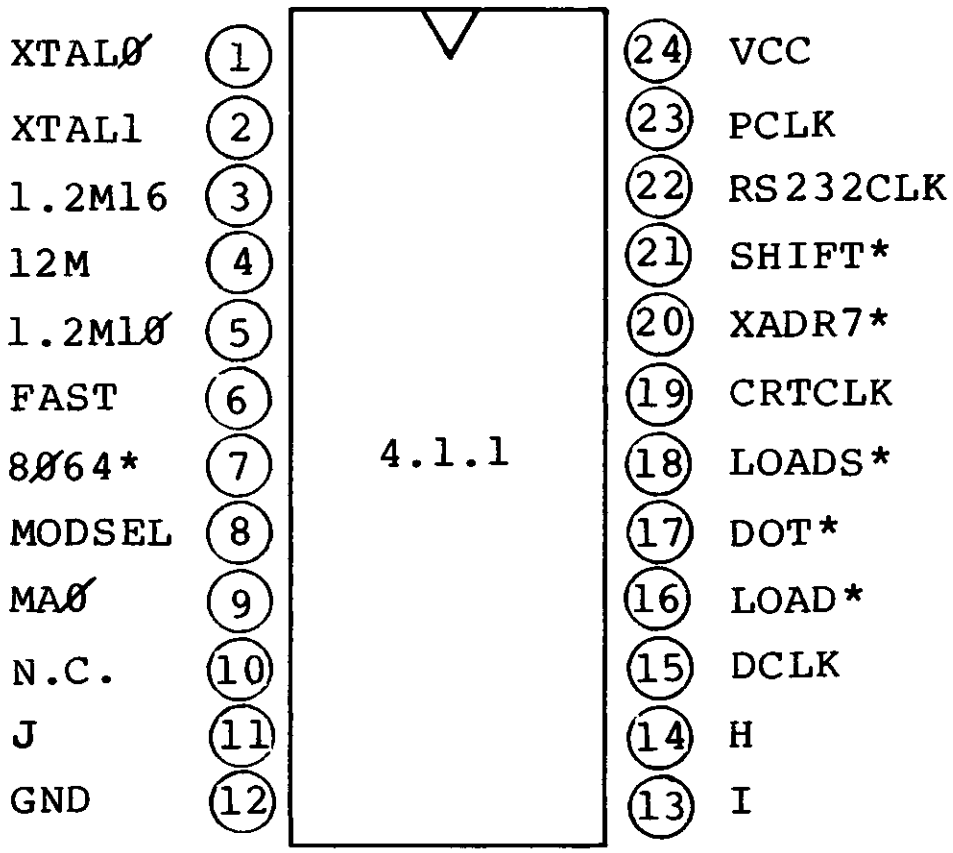
MAX. CLOCK FREQ.: 20.2752 MHz

OPER TEMP.: Ø° C to 7Ø° C

OPERATING VOLTAGE & RANGE: 5 V ± 5%

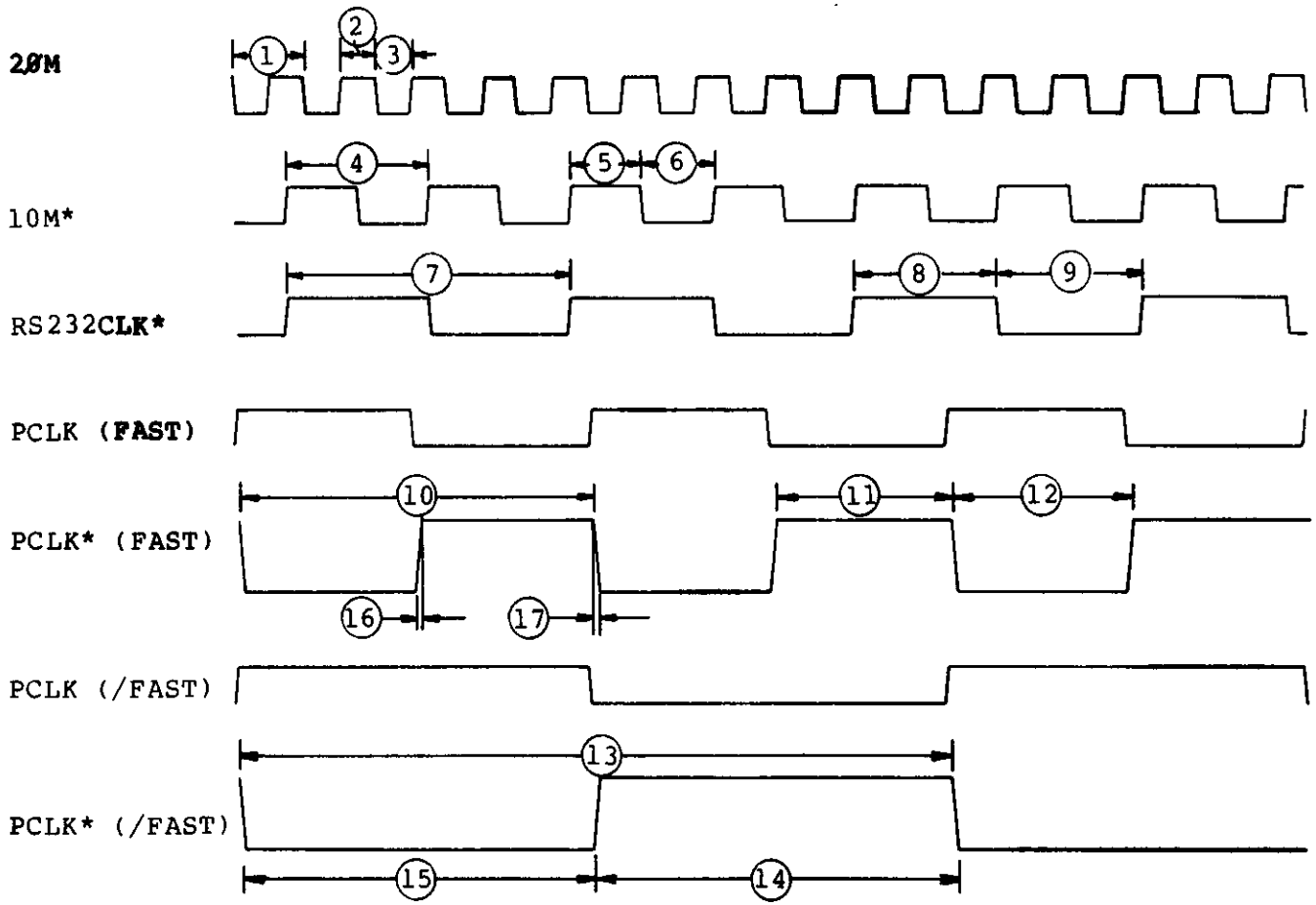

20.2752
MHZ
CRYSTAL
OSC.
PCLK
RS232CLK
1.2672MHZ
÷
16
PLL
NE564
12.672MHZ
SHIFT*
XADR7*
CRTCLK
LOADS*
÷
10
1.2672MHZ
DDT*
FAST
LOAD*
DCLK
8Ø64*
H
MODSEL
I
MAØ
J

24 PIN CHIP


XTALØ 1
XTAL1 2
1.2M16 3
12M 4
1.2M1Ø 5
FAST 6
8Ø64* 7
MODSEL 8
MAØ 9
N.C. 10
J 11
GND 12
4.1.1
24 VCC
23 PCLK
22 RS232CLK
21 SHIFT*
20 XADR7*
19 CRTCLK
18 LOADS*
17 DOT*
16 LOAD*
15 DCLK
14 H
13 I

SYSTEM TIMING SPECS

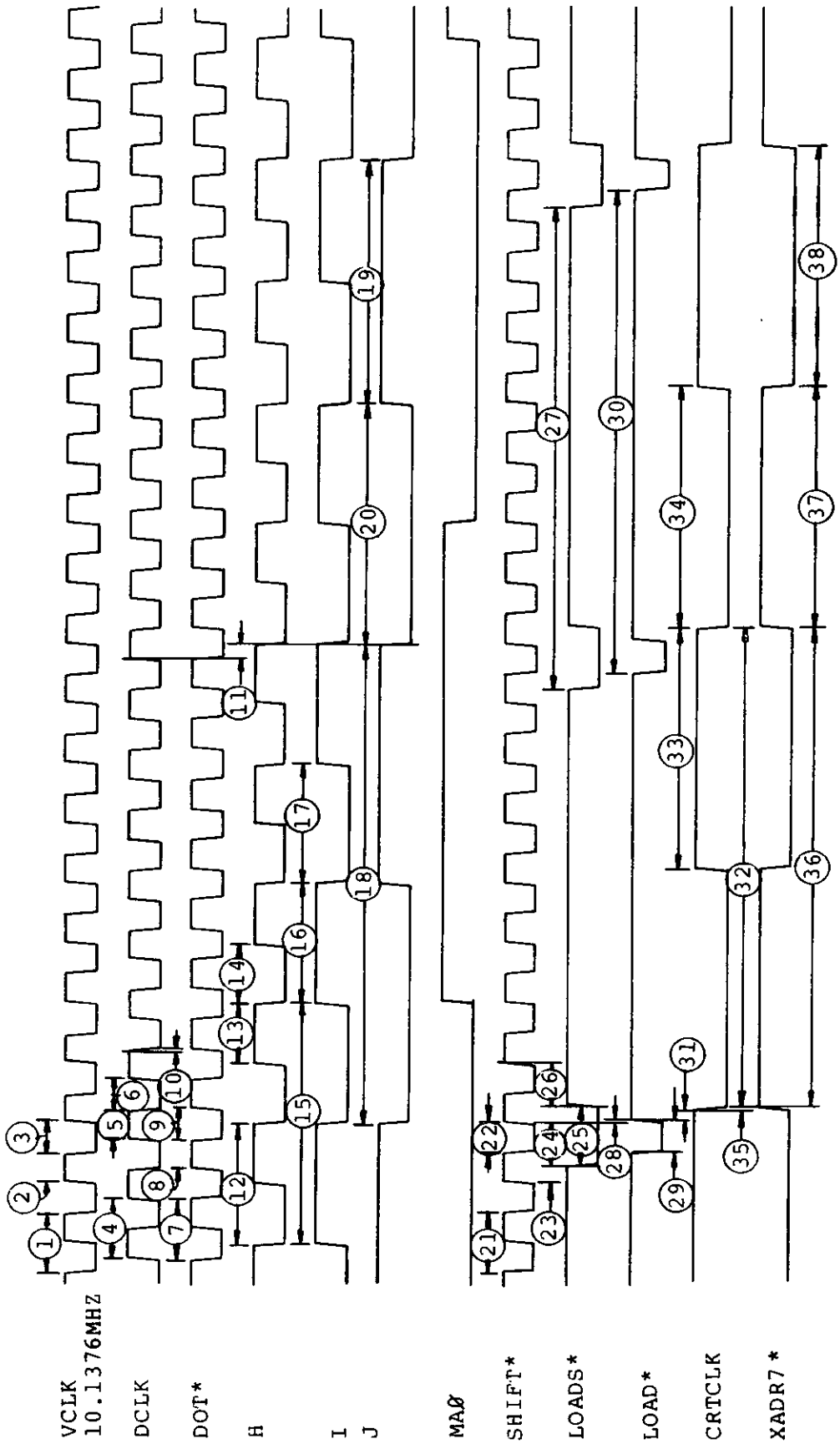
NUMBER	PARAMETER	MIN.	TYP.	MAX.	UNITS
1	20M Cycle Time		49.3		ns
2	20M Pulse Width (High)	20			ns
3	20M Pulse Width (Low)	20			ns
4	$\overline{10M}$ Cycle Time		98.6		ns
5	$\overline{10M}$ Pulse Width (High)	45 40			ns
6	$\overline{10M}$ Pulse Width (Low)	45 40			ns
7	$\overline{RS232CLK}$ Cycle Time		197.2		ns
8	$\overline{RS232CLK}$ Pulse Width (High)	92			ns
9	$\overline{RS232CK}$ Pulse Width (Low)	92			ns
10	PCLK* (Fast) Cycle Time		246.6		ns
11	PCLK* (Fast) Pulse Width (High)	110			ns
12	PCLK* (Fast) Pulse Width (Low)	110			ns
13	PCLK* (/Fast) Cycle Time		493.2		ns
14	PCLK* (/Fast) Pulse Width (High)	180			ns
15	PCLK* (/Fast) Pulse Width (Low)	180			ns
16	PCLK* Rise Time			13	ns
17	PCLK* Fall Time			13	ns
	DC CHARACTERISTICS (ALL PINS)				
–	Input Voltage Level (High)	2.0			V
–	Input Voltage Level (Low)			.8	V
–	Output Voltage Level (High)	2.8	3.5		V
–	Output Voltage Level (Low)		.35	.5	V
	(ALL PINS EXCEPT CRTCLK OUTPUT)				
–	Input Current Level (High)			40	μa
–	Input Current Level (Low)			−1.6	ma
–	Output Current Level (High)	−160			μa
–	Output Current Level (Low)	3.2			ma
	(CRTCLK OUTPUT)				
–	Output Current Level (High)	−400			μa
–	Output Current Level (Low)	8			ma



SYSTEM TIMING

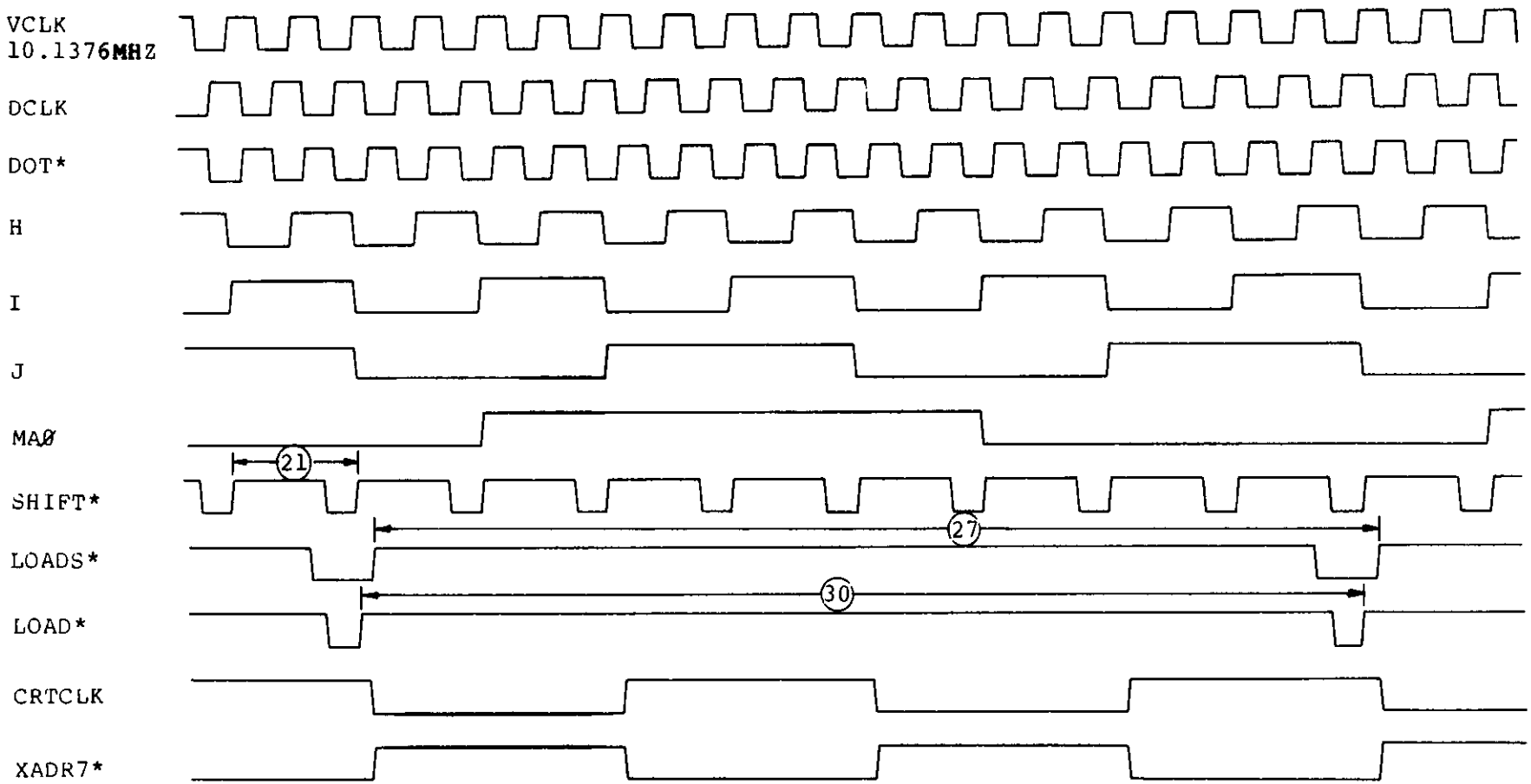
VIDEO TIMING SPECS

		10.1376 MHz			12.672 MHz			
NUMBER	PARAMETER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
1	VCLK Cycle Time		98.6			78.9		ns
2	VCLK Pulse Width (High)	40			30			ns
3	VCLK Pulse Width (Low)	40			30			ns
4	DCLK Cycle Time		98.6			78.9		ns
5	DCLK Pulse Width (High)	40			30			ns
6	DCLK Pulse Width (Low)	40			30			ns
7	$\overline{\text{DOT}}$ Cycle Time		98.6			78.9		ns
8	$\overline{\text{DOT}}$ Pulse Width (High)	40			30			ns
9	$\overline{\text{DOT}}$ Pulse Width (Low)	40			30			ns
10	DCLK ↓ to $\overline{\text{DOT}}$ ↑			5			5	ns
11	DCLK ↑ to H, I, J ↑↓			27			27	ns
12	H Cycle Time		197.2			157.8		ns
13	H Pulse Width (High)	90			70			ns
14	H Pulse Width (Low)	90			70			ns
15	I Cycle Time		394.4			315.6		ns
16	I Pulse Width (High)	190			150			ns
17	I Pulse Width (Low)	190			150			ns
18	J Cycle Time		788.8			631.2		ns
19	J Pulse Width (High)	385			305			ns
20	J Pulse Width (Low)	385			305			ns
21	$\overline{\text{SHIFT}}$ Cycle Time							
	(64x16 & 80x24 Mode)		98.6			78.9		ns
	(32x16 & 40x24 Mode)		197.2			157.8		ns
22	$\overline{\text{SHIFT}}$ Pulse Width (Low)	30			30			ns
23	$\overline{\text{SHIFT}}$ ↑ to $\overline{\text{LOADS}}$ ↓	0		27*	0		27*	ns
24	$\overline{\text{LOADS}}$ ↓ to $\overline{\text{SHIFT}}$ ↑	50*			50*			ns
25	$\overline{\text{LOADS}}$ Pulse Width (Low)	70	98.6		70	78.9		ns
26	$\overline{\text{LOADS}}$ ↑ to $\overline{\text{SHIFT}}$ ↑	50*			50*			ns
27	$\overline{\text{LOADS}}$ Cycle Time							
	(64x16 & 80x24 Mode)		788.8			631.2		ns
	(32x16 & 40x24 Mode)		1577.6			1262.4		ns
28	$\overline{\text{SHIFT}}$ ↑ to $\overline{\text{LOAD}}$ ↑			5			5	ns
29	$\overline{\text{LOAD}}$ Pulse Width (Low)	40			30			ns
30	$\overline{\text{LOAD}}$ Cycle Time							
	(64x16 & 80x24 Mode)		788.8			631.2		ns
	(32x16 & 40x24 Mode)		1577.6			1262.4		ns
31	$\overline{\text{LOAD}}$ ↑ to CRTCLK ↓	0		27	0		27	ns
32	CRTCLK Cycle Time		788.8			631.2		ns
33	CRTCLK Pulse Width (High)	385			305			ns
34	CRTCLK Pulse Width (Low)	385			305			ns
35	CRTCLK ↑↓ to $\overline{\text{XADR7}}$ ↓↑			5			5	ns
36	$\overline{\text{XADR7}}$ Cycle Time		788.8			631.2		ns
37	$\overline{\text{XADR7}}$ Pulse Width (High)	385			305			ns
38	$\overline{\text{XADR7}}$ Pulse Width (Low)	385			305			ns



VIDEO TIMING

64 X 16 MODE
80 X 24 MODE



VIDEO TIMING

32 X 16 MODE
40 X 24 MODE

4.1

PIN	SIGNAL	MAX. CAPACITANCE
23	PCLK	35 pf
22	RS232CK	105 pf
21	SHIFT*	35 pf
20	XADR7*	35 pf
19	CRTCLK	35 pf
18	LOADS*	35 pf
17	DOT*	35 pf
16	LOAD*	35 pf
15	DCLK	35 pf
14	H	35 pf
13	I	35 pf
11	J	35 pf

ARRAY #: 4.2.1

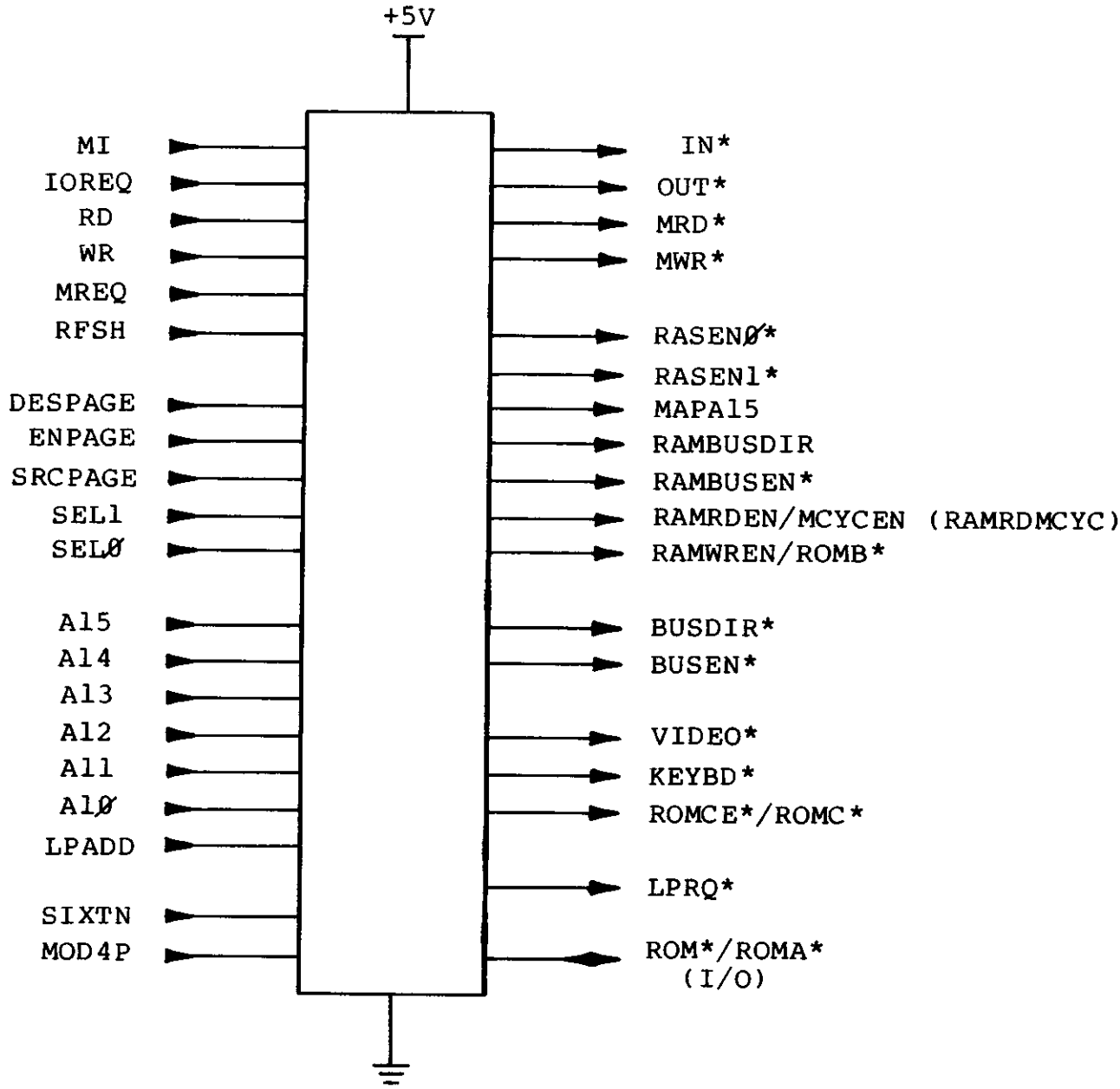
CIRCUIT NAME: Address Decode

NO. OF PINS: 40

MAX. CLOCK FREQ.: 4 MHz

OPER. TEMP.: 0° C to 70° C

OPERATING VOLTAGE & RANGE: 5 ± 5%

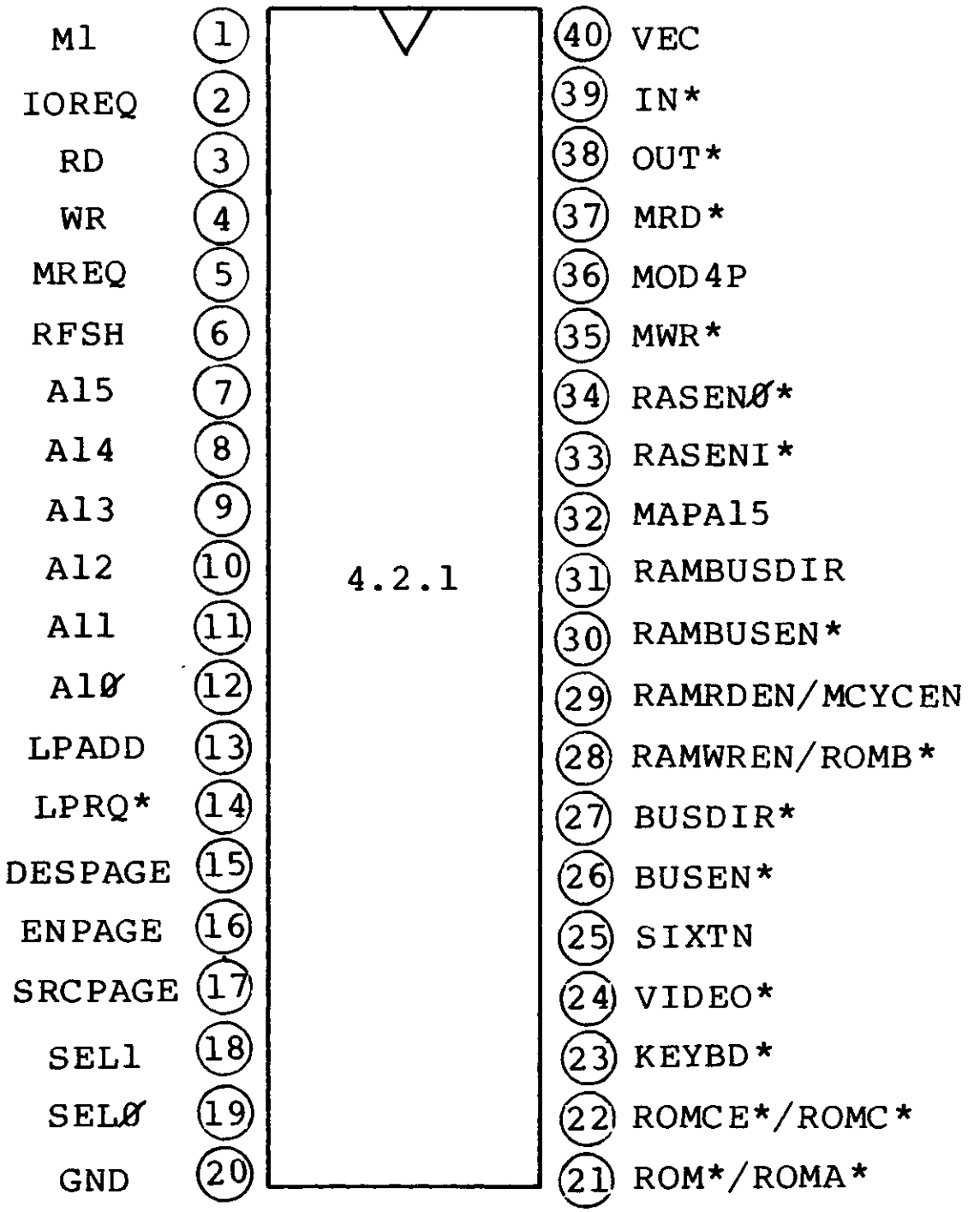


40 PINS USED

40 PIN CHIP

4.2.0

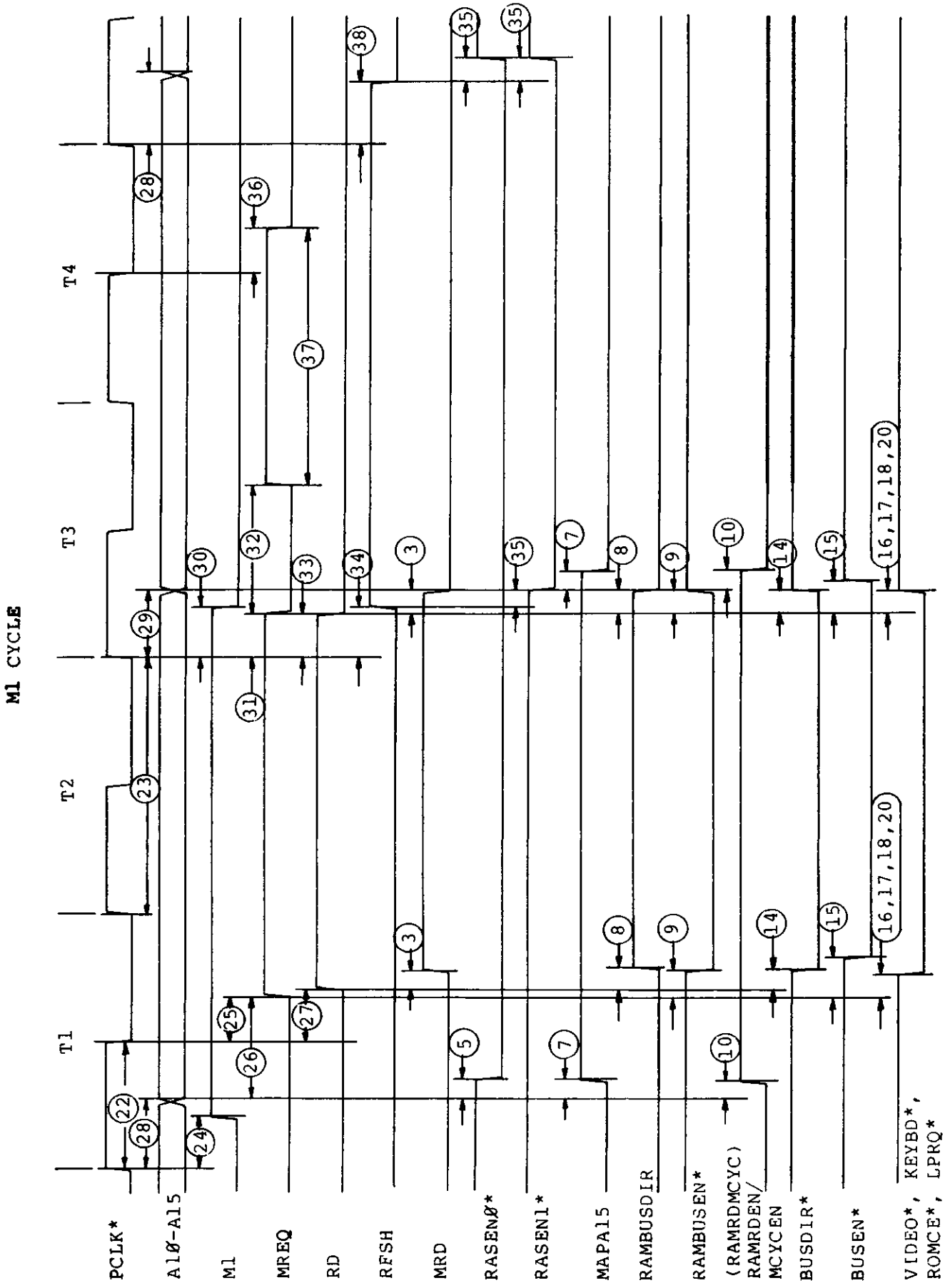
ADDRESS DECODE


M1 1
IOREQ 2
RD 3
WR 4
MREQ 5
RFSH 6
A15 7
A14 8
A13 9
A12 10
A11 11
A10 12
LPADD 13
LPRQ* 14
DESPAGE 15
ENPAGE 16
SRCPAGE 17
SEL1 18
SEL0 19
GND 20
4.2.1
40 VEC
39 IN*
38 OUT*
37 MRD*
36 MOD4P
35 MWR*
34 RASEN0*
33 RASENI*
32 MAPA15
31 RAMBUSDIR
30 RAMBUSEN*
29 RAMRDEN/MCYCEN
28 RAMWREN/ROMB*
27 BUSDIR*
26 BUSEN*
25 SIXTN
24 VIDEO*
23 KEYBD*
22 ROMCE*/ROMC*
21 ROM*/ROMA*

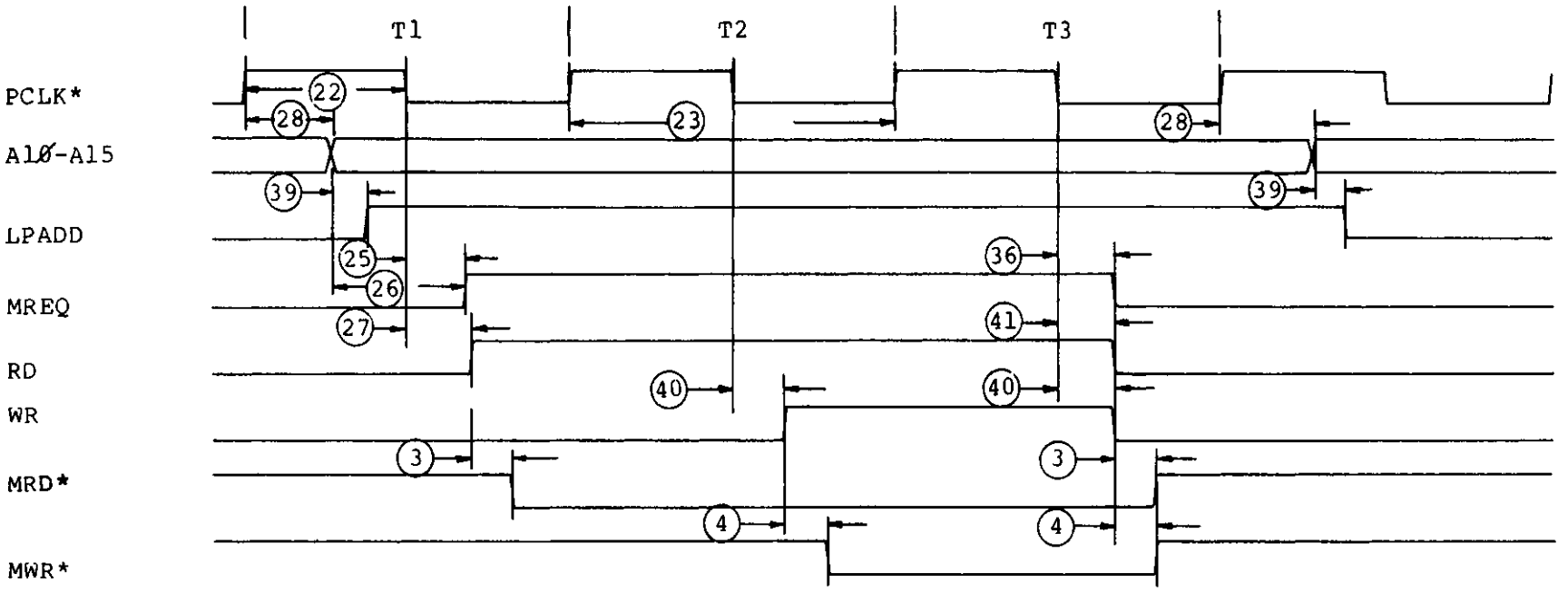
SIGNAL NAME	MODEL A MODE		MODEL 4 MODE	
MDD4P	"1" = +5V		"0" = GND	
MI	MI	I	MI	I
IOREQ	IOREQ	I	IOREQ	I
RD	RD	I	RD	I
WR	WR	I	WR	I
MREQ	MREQ	I	IOREQ	I
RFSH	RFSH	I	RFSH	I
DESPAGE	DESPAGE	I	DESPAGE	I
ENPAGE	ENPAGE	I	ENPAGE	I
SRCPAGE	SRCPAGE	I	SRCPAGE	I
SEL1	SEL1	I	SEL1	I
SEL0	SEL0	I	SEL0	I
A15	A15	I	A15	I
A14	A14	I	A14	I
A13	A13	I	A13	I
A12	A12	I	A12	I
A11	A11	I	A11	I
A10	A10	I	A10	I
LPADD	LPADD	I	LPADD	I
SIXTN	SIXTN	I	SIXTN	I
IN*	IN*	O	IN*	O
OUT*	OUT*	O	OUT*	O
MRD*	MRD*	O	MRD*	O
MWR*	MWR*	O	MWR*	O
RASEN0*	RASEN0*	O	RASEN0*	O
RASEN1*	RASEN1*	O	RASEN1*	O
MAPA15	MAPA15	O	MAPA15	O
RAMBUSDIR	RAMBUSDIR	O	RAMBUSDIR	O
RAMBUSEN*	RAMBUSEN*	O	RAMBUSEN*	O
(RAMRDMCYC) RAM RDEN/MCYCEN	RAMRDEN	O	MCYCEN	O
RAM WREN/ROMB*	RAMWREN	O	ROMB*	O
BUSDIR*	BUSDIR*	O	BUSDIR*	O
BUSEN*	BUSEN4P*	O	DATACNT*	O
VIDEO*	VIDEO4P*	O	VIDEO4*	O
KEYBD*	KEYBD4P*	O	KEYBD4*	O
ROMCE*/ROMC*	ROMCE*	O	ROMC*	O
LPRQ*	LPRQ*	O	LPRQ*	O
ROM*/ROMA*	ROM*	I	ROMA*	O

I = INPUT
O = OUTPUT

		SPECS			
	PARAMETER	MIN.	TYP.	MAX.	UNITS
1	IOREQ ↑↓ * RD ↑↓ to $\overline{IN}$ ↓↑			35	ns
2	IOREQ ↑↓ * WR ↑↓ to $\overline{OUT}$ ↓↑			35	ns
3	RD ↑↓ to $\overline{MRD}$ ↓↑			35	ns
4	WR ↑↓ to $\overline{MWR}$ ↓↑			35	ns
5	A15 ↑↓ to RASEN0 ↑↓			50	ns
6	A15 ↑↓ to RASEN1 ↑↓			50	ns
7	A15 ↑↓ to MAPA15 ↑↓			50	ns
8	RD ↓↑ to RAMBUSDIR ↓↑			35	ns
9	MREQ ↑↓ to $\overline{RAMBUSEN}$ ↓↑			35	ns
10	A15–A10 ↑↓ to RAMRDMCYC ↑↓			50	ns
11	A15–A14 ↑↓ to RAMWREN ↑↓			50	ns
12	MREQ ↑↓ to $\overline{ROMB}$ ↓↑			35	ns
13	IOREQ ↑↓ to $\overline{BUSDIR}$ ↓↑			35	ns
14	RD ↑↓ to $\overline{BUSDIR}$ ↓↑			35	ns
15	MREQ ↑↓ to $\overline{BUSEN}$ ↓↑			50	ns
16	MREQ ↑↓ to $\overline{VIDEO}$ ↓↑			35	ns
17	MREQ ↑↓ to $\overline{KEYBD}$ ↓↑			35	ns
18	MREQ ↑↓ to $\overline{ROMCE}$ ↓↑			35	ns
19	MREQ ↑↓ to $\overline{ROMC}$ ↓↑			35	ns
20	MREQ ↑↓ to $\overline{LPRQ}$ ↓↑			35	ns
21	MREQ ↑↓ to $\overline{ROMA}$ ↓↑			35	ns
22	$\overline{PCLK}$ ↑↓ to $\overline{PCLK}$ ↓↑	110	123		ns
23	PCLK Cycle Time		246		ns
24	$\overline{PCLK}$ ↑ to M1 ↑			106	ns
25	$\overline{PCLK}$ ↓ to MREQ ↑			91	ns
26	A10–A15 ↑↓ to MREQ ↑	50			ns
27	$\overline{PCLK}$ ↓ to RD ↑			101	ns
28	$\overline{PCLK}$ ↑ to A10–A15 ↑↓			128	ns
29	$\overline{PCLK}$ ↑ to A10–A15 ↑↓			128	ns
30	$\overline{PCLK}$ ↑ to M1 ↓			136	ns
31	$\overline{PCLK}$ ↑ to MREQ ↓			91	ns
32	MREQ ↓ to MREQ ↑	110			ns
33	$\overline{PCLK}$ ↑ to RD ↓			91	ns
34	$\overline{PCLK}$ ↑ to RFSH ↑			136	ns
35	RFSH ↑↓ to $\overline{RASEN0}$ or $\overline{RASEN1}$ ↑↓			35	ns
36	$\overline{PCLK}$ ↓ to MREQ ↓			91	ns
37	MREQ Pulse Width (High)	220		126	ns
38	$\overline{PCLK}$ ↑ to RFSH ↓				
39	A1–A9 ↑↓ to LPADD ↑↓			30	ns
40	$\overline{PCLK}$ ↓ to WR ↑↓			86	ns
41	$\overline{PCLK}$ ↓ to RD ↓			91	ns
42	Control Lines ↑↓ to Affected Signals ↑↓			35	ns
43	A0–A15 ↑↓ to IOREQ ↑	200			ns
44	$\overline{PCLK}$ ↑ to IOREQ ↑			81	ns
45	$\overline{PCLK}$ ↑ to RD ↑			91	ns
46	$\overline{PCLK}$ ↑ to WR ↑			71	ns

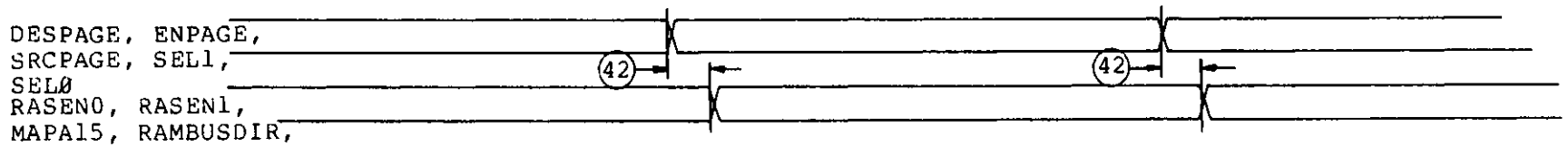

M1 CYCLE
T1
T2
T3
T4
PCLK*
A1Ø-A15
M1
MREQ
RD
RFSH
MRD
RASENØ*
RASEN1*
MAPA15
RAMBUSDIR
RAMBUSEN*
(RAMRDMCYC)
RAMRDEN/
MCYCEN
BUSDIR*
BUSEN*
VIDEO*, KEYBD*,
ROMCE*, LPRQ*
ROMA*, ROMB*, ROMC*

READ OR WRITE CYCLE

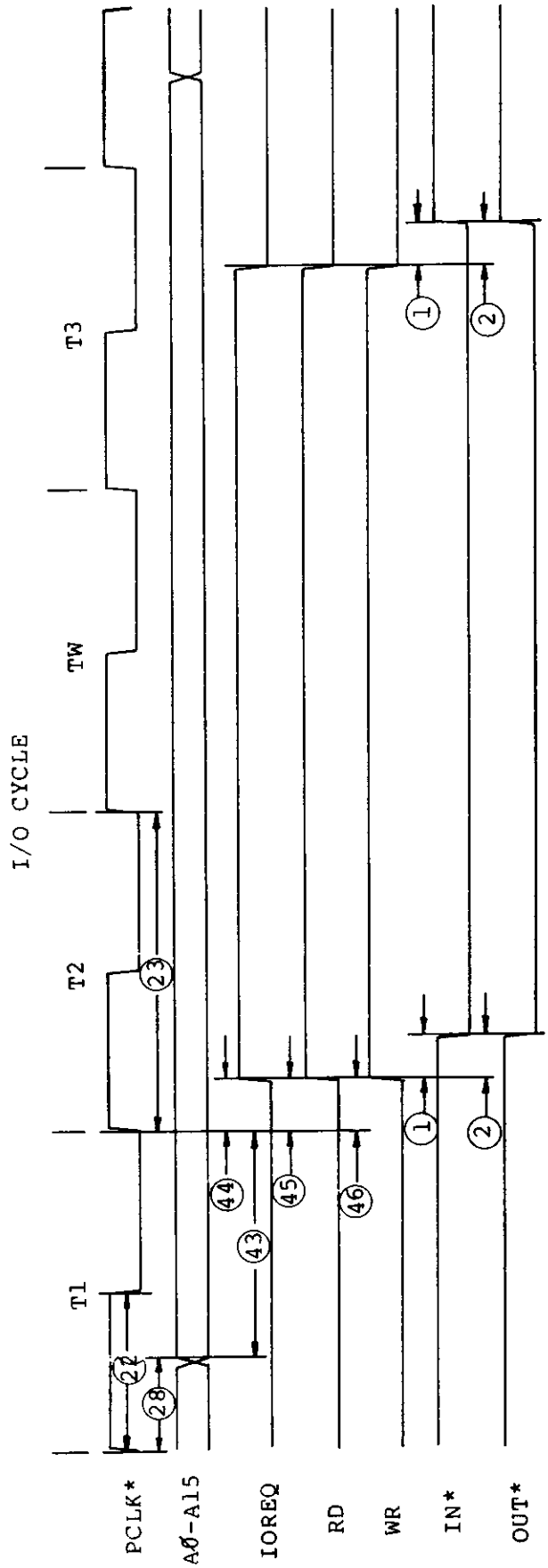


RASEN0, RASEN1, MAPA15, RAMBUSDIR, RAMBUSEN*, RAMRDMCYC, BUSDIR*, BUSEN*, VIDEO*, KEYBD*, ROMCE*, LPRQ, ROMA*, ROMB*, ROMC* - Refer to M1 Cycle

CONTROL LINES



DESPAGE, ENPAGE,
SRCPAGE, SEL1,
SELØ
RASEN0, RASEN1,
MAPA15, RAMBUSDIR,
RAMBUSEN*, RAMRDMCYC,
RAMWREN, ROMB*,
BUSEN*, VIDEO*,
KEYBD*, ROMCE*,
ROMC*, LPRQ*,
ROMA*


I/O CYCLE
T1
T2
TW
T3
PCLK*
A0-A15
IOREQ
RD
WR
IN*
OUT*
22
23
28
43
44
45
46
1
2
1
2

DC CHARACTERISTICS (ALL PINS) 0° – 70° C

PARAMETER	MIN.	TYP.	MAX.	UNITS
Input Voltage Level (High)	2.0			V
Input Voltage Level (Low)			.8	V
Output Voltage Level (High)	2.7	3.5		V
Output Voltage Level (Low)		.35	.5	V
(ALL PINS EXCEPT OUT*, RAMRDEN/MCYCEN)				
Input Current Level (High)			20	μa
Input Current Level (Low)			−.4	ma
Output Current Level (High)	−200			μa
Output Current Level (Low)	4			ma
(OUT*, RAMRDEN/MCYCEN)				
Output Current Level (High)	−400			μa
Output Current Level (Low)	8			ma

	PIN	SIGNAL	MAX. CAPACITANCE
	39	IN*	35 pf
	38	OUT*	35 pf
	37	MRD*	35 pf
	35	MWR*	128 pf
	34	RASENØ*	35 pf
	33	RASEN1*	35 pf
	32	MAPA15	35 pf
	31	RAMBUSDIR	35 pf
	30	RAMBUSEN*	35 pf
	29	RAMRDEN/MCYCEN	35 pf
	28	RAMWREN/ROMB*	35 pf
	27	BUSDIR*	35 pf
	26	BUSEN*	35 pf
	24	VIDEO*	35 pf
	23	KEYBD*	35 pf
	22	ROMCE*/ROMC*	35 pf
(OUTPUT)	21	ROMA*	35 pf
	14	LPRQ*	35 pf

ARRAY #: 4.3.Ø

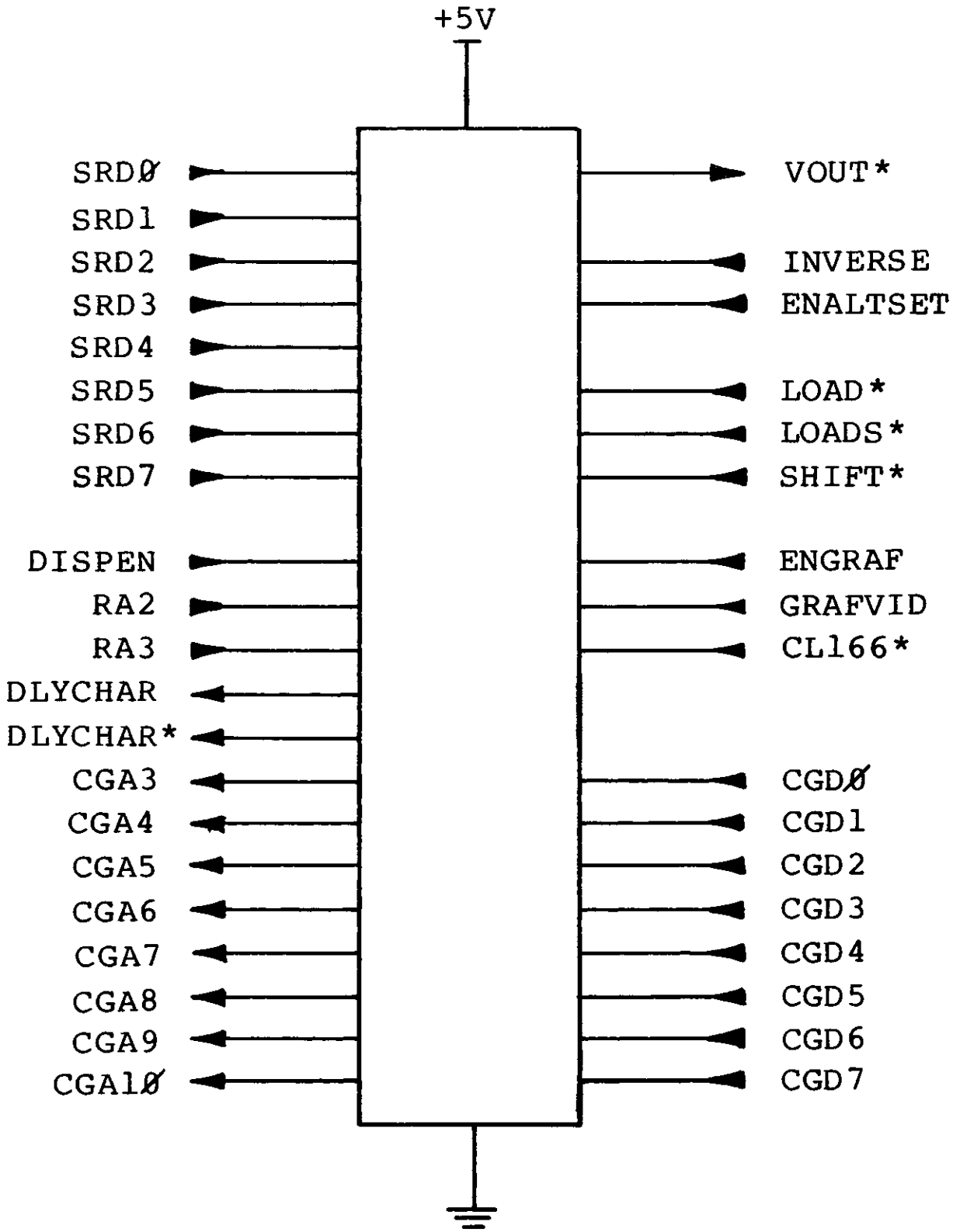
CIRCUIT NAME: Video Support

NO. OF PINS: 4Ø

MAX. CLOCK FREQ.: 12.672 MHz

OPER. TEMP.: Ø° C to 7Ø° C

OPERATING VOLTAGE & RANGE: 5 ± 5%

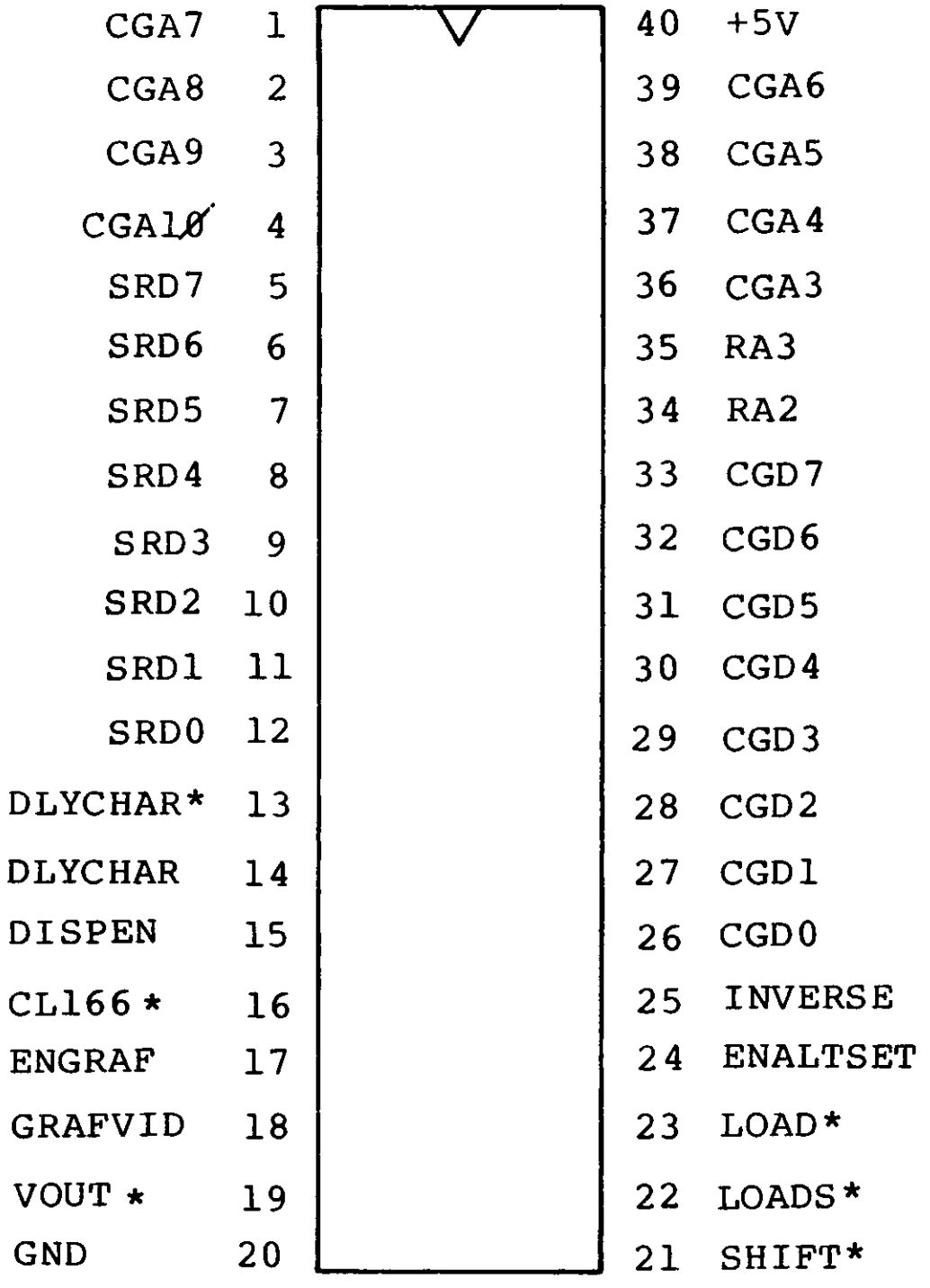


39 PINS USED

40 PIN CHIP

4.3.Ø

VIDEO SUPPORT

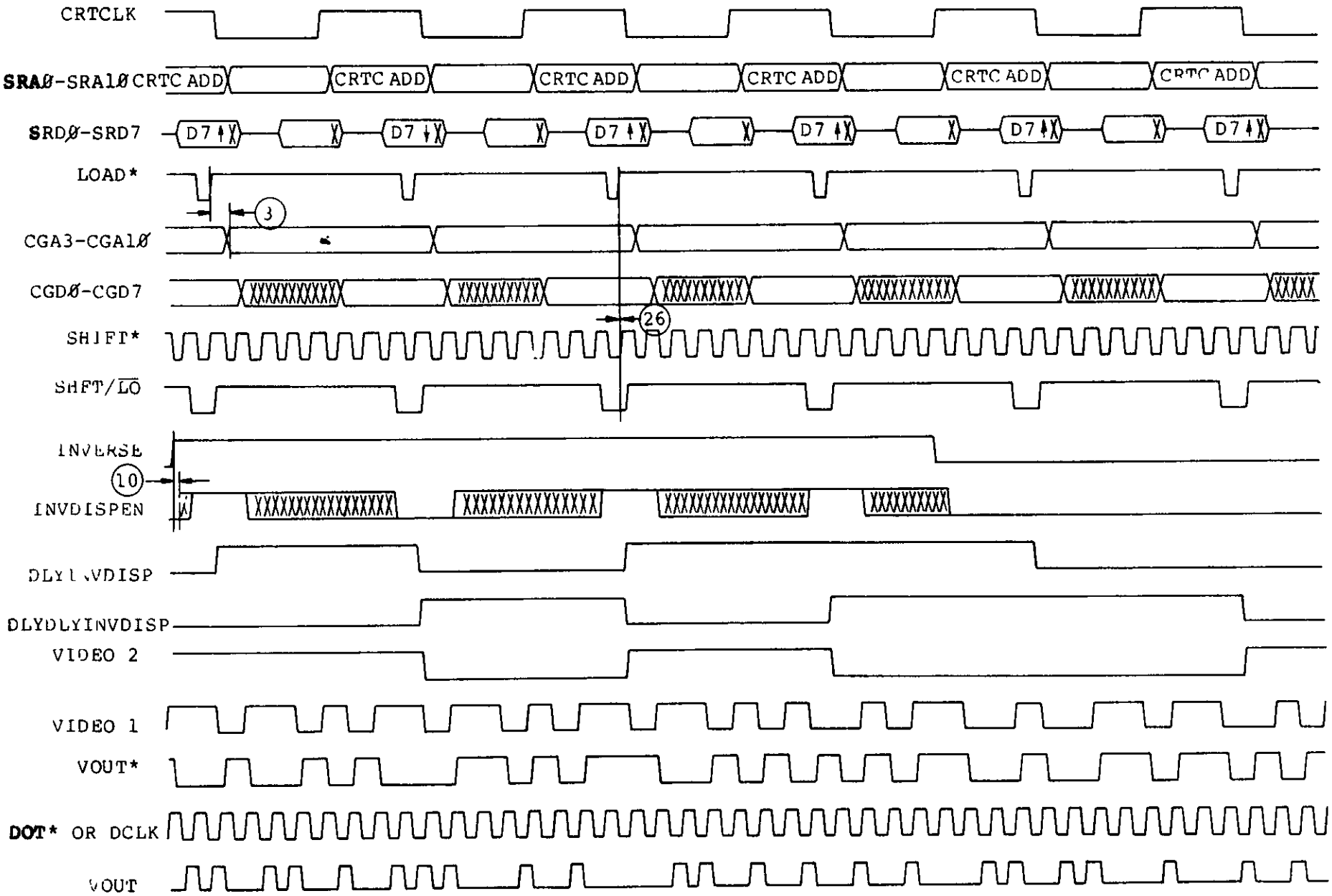

CGA7 1
CGA8 2
CGA9 3
CGA10 4
SRD7 5
SRD6 6
SRD5 7
SRD4 8
SRD3 9
SRD2 10
SRD1 11
SRD0 12
DLYCHAR* 13
DLYCHAR 14
DISPEN 15
CL166* 16
ENGRAF 17
GRAFVID 18
VOUT* 19
GND 20
40 +5V
39 CGA6
38 CGA5
37 CGA4
36 CGA3
35 RA3
34 RA2
33 CGD7
32 CGD6
31 CGD5
30 CGD4
29 CGD3
28 CGD2
27 CGD1
26 CGD0
25 INVERSE
24 ENALTSET
23 LOAD*
22 LOADS*
21 SHIFT*

	PARAMETER	MIN.	TYP.	SPECS MAX.	UNITS
1**	SRD0–SRD7 ↑↓ to $\overline{\text{LOAD}}$ ↑	61			ns
2*	Inputs D0–D7 of LS273 ↑↓ to $\overline{\text{LOAD}}$ ↑	20			ns
3	$\overline{\text{LOAD}}$ ↑ to CGA3–CGA10 ↑↓	0		60	ns
4	RA2, RA3 ↑↓ to Outputs of LS153 ↑↓	0		38	ns
5	Inputs CGA3–CGA10 of LS153 ↑↓ to Outputs ↑↓	0		30	ns
6	$\overline{\text{DLYGRAPHIC}}$ ↓ to Outputs of LS244 ↑↓	0		30	ns
7	$\overline{\text{DLYGRAPHIC}}$ ↑ to Outputs of LS244 Tristate	0		30	ns
8	ENALTSET ↑↓ to CGA9 ↑↓	0		35	ns
9	INVERSE ↑↓ to Inputs D7 of LS273 ↑↓	0		35	ns
10	INVERSE ↑↓ to INVDISPEN, CHAR ↑↓	0		40	ns
11	INVERSE ↑↓ to Input to 51 ↑↓	0		20	ns
12	SRD6 ↑↓ to CHAR ↑↓	0		40	ns
13	DISPEN ↑↓ to Input D0 of LS175 ↑↓	0		20	ns
14	DISPEN ↑↓ to INVDISPEN ↑↓	0		40	ns
15	ENGRAF ↑↓ to INVDISPEN ↑↓	0		40	ns
16	ENGRAF ↑↓ to Inputs of 51 ↑↓	0		20	ns
17	GRAFVID ↑↓ to Input of 51 ↑↓	0		5	ns
20**	CGD0–CGD7 ↑↓ to LOADS ↓ & SHIFT ↑	100			ns
21	RA3 ↑↓ to DLYBLANK ↑↓ 0	27		50	ns
22	$\overline{\text{LOAD}}$ ↑ to DLYBLANK ↑↓ 0	27		50	ns
23**	$\overline{\text{LOADS}}$ ↓ to $\overline{\text{SHIFT}}$ ↑	50			ns
24*	$\overline{\text{SHFT/LD}}$ ↓ to $\overline{\text{SHIFT}}$ ↑	30			ns
25	$\overline{\text{CL166}}$ ↑↓ to QH ↑↓	0		30	ns
26*	$\overline{\text{LOAD}}$ ↑ to $\overline{\text{SHIFT}}$ ↑			± 5	ns
27[1]	$\overline{\text{LOAD}}$ ↑ to VIDEO2 ↑↓ = $\overline{\text{SHIFT}}$ ↑ to VIDEO1 ↑↓			± 5	ns
28	GRAFVID ↑↓ to VIDEO2 ↑↓	0		15	ns
29	VIDEO2 ↑↓, VIDEO1 ↑↓ to $\overline{\text{VOUT}}$ ↑↓	0		20	ns
30	ENGRAF ↑↓ to VIDEO2 ↑↓	0		15	ns
31	DLYCHAR* ↑ to CGD0–CGD7 Tristate			150	ns
32	CRTCLK ↓ to DISPEN			300	ns

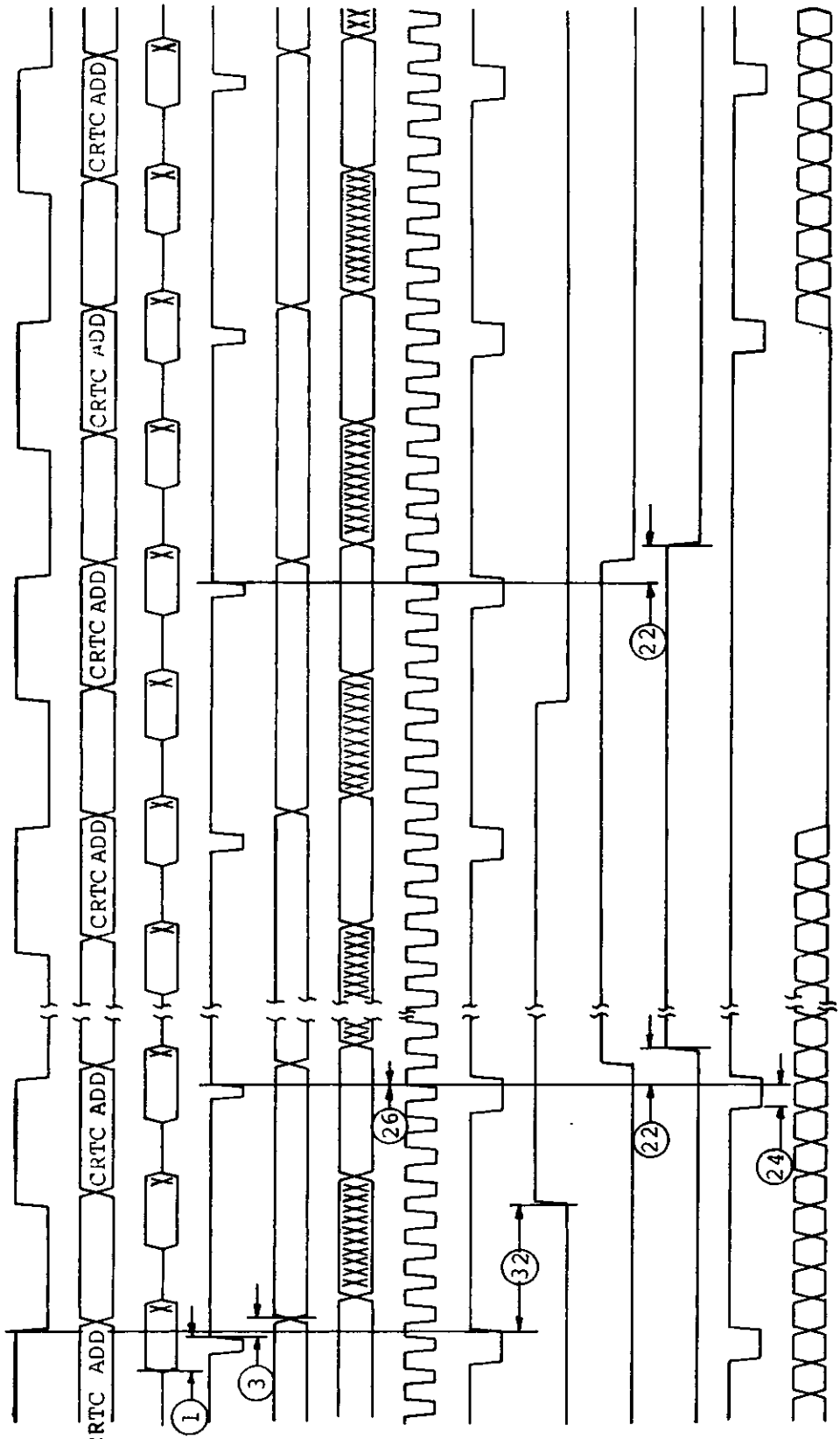
[1] The delay from $\overline{\text{LOAD}}$ ↑ to VIDEO2 ↑↓ should equal the delay from $\overline{\text{SHIFT}}$ ↑ to VIDEO1 ↑↓.

* Specs required for TLL components—can be changed to meet the setup & hold time specs of array logic.

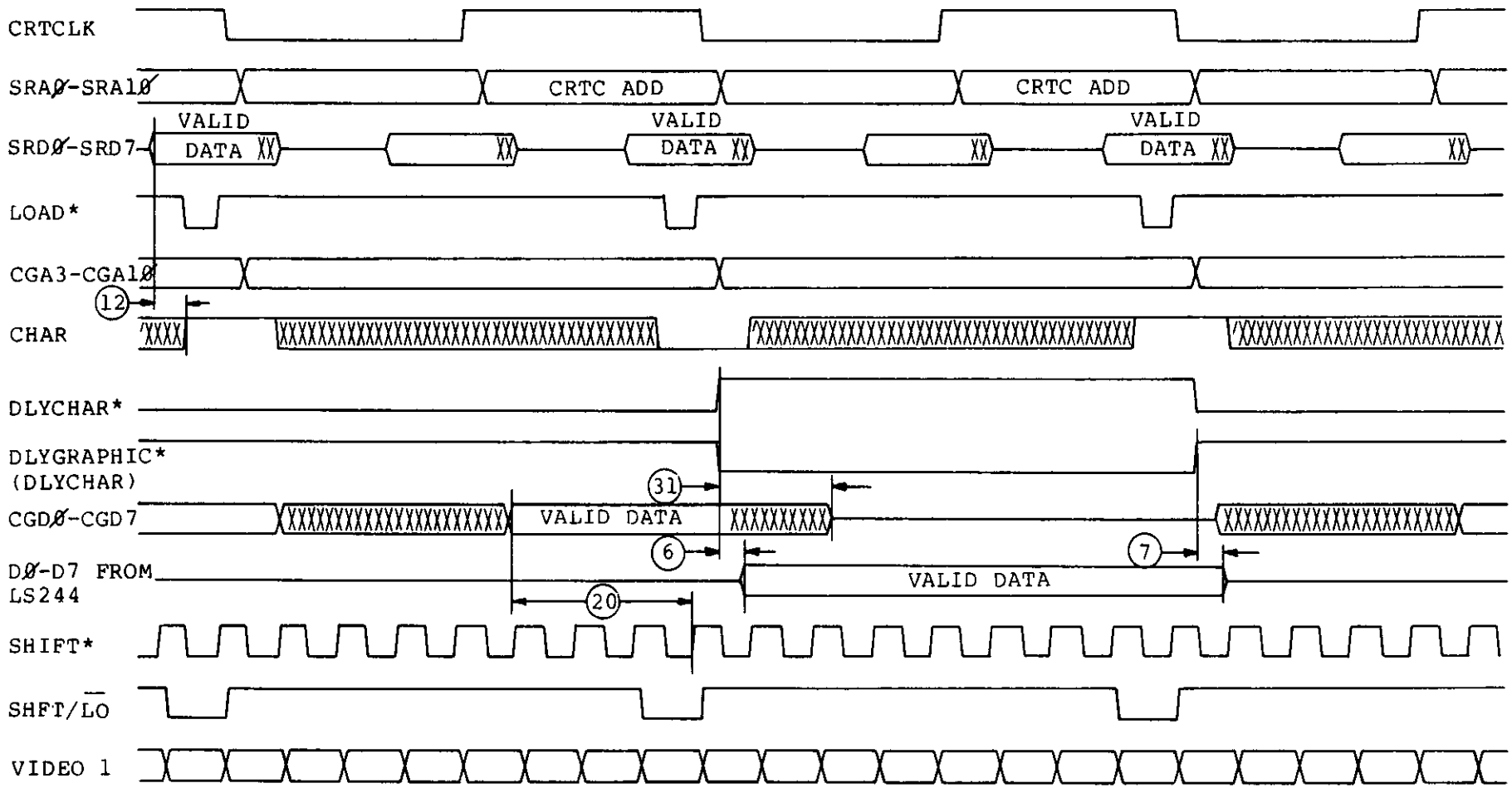
** Specs provided are for reference, timing is from external logic.



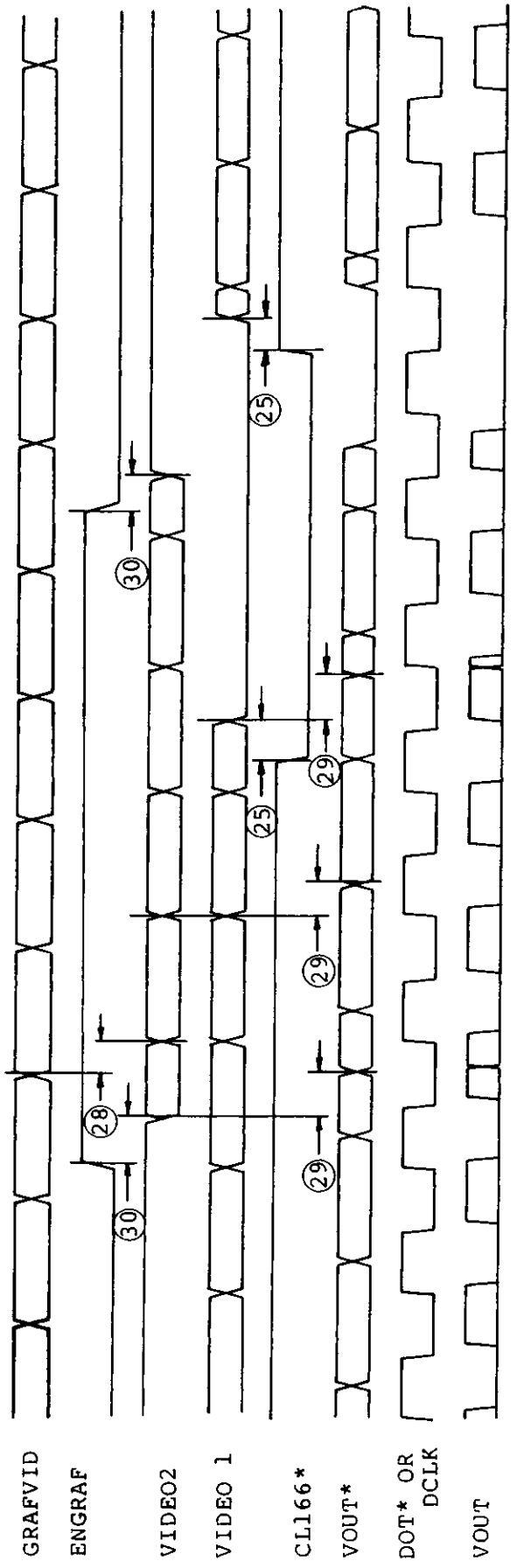
INVERSE VIDEO TIMING


CRTCLK
SRAØ-SRA1Ø
SRDØ-SRD7
LOAD*
CGA3-CGA1Ø
CGDØ-CGD7
SHIFT*
LOADS*
DISPEN
DLYDISPEN
DLYBLANK
SHFT/LD
VIDEO 1
CRTC ADD
1
3
26
32
22
22
24

BLANKING

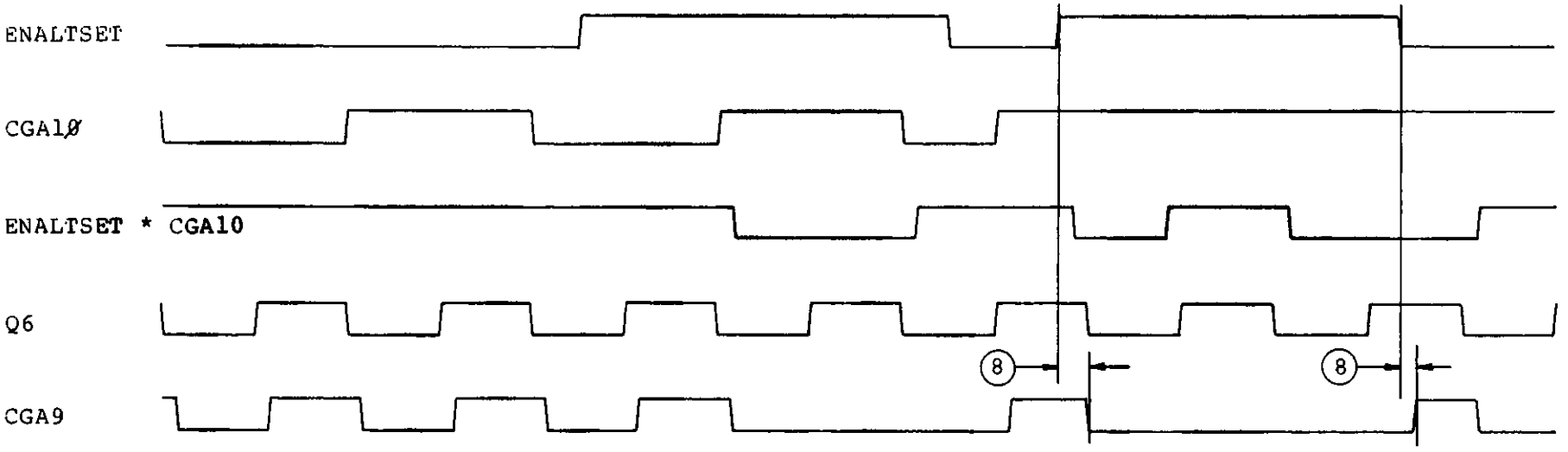


DLYCHAR* & DLYGRAPHIC* CONTROL



GRAFVID, ENGRAF, CL166*, VIDEO1

RELATIONSHIP



ENALTSET	CGA10	Q6	CGA9
Ø	Ø	Ø	Ø
Ø	Ø	1	1
Ø	1	Ø	Ø
Ø	1	1	1
1	Ø	Ø	Ø
1	Ø	1	1
1	1	Ø	Ø
1	1	1	Ø

ENALTSET CONTROL

DC CHARACTERISTICS (ALL PINS) Ø° – 7Ø° C

PARAMETER	MIN.	TYP.	MAX.	UNITS
Input Voltage Level (High)	2.Ø			V
Input Voltage Level (Low)			.8	V
Output Voltage Level (High)	2.7	3.5		V
Output Voltage Level (Low)		.35	.5	V
Input Current Level (High)			2Ø	µa
Input Current Level (Low)			–.4	ma
Output Current Level (High)	–2ØØ			µa
Output Current Level (Low)	4			ma

PIN	SIGNAL	MAX. CAPACITANCE
4	CGA1Ø	35 pf
3	CGA9	35 pf
2	CGA8	35 pf
1	CGA7	35 pf
39	CGA6	35 pf
38	CGA5	35 pf
37	CGA4	35 pf
36	CGA3	35 pf
13	DLYCHAR*	35 pf
14	DLYCHAR	35 pf
19	VOUT*	35 pf

ARRAY #: 4.4.Ø

CIRCUIT NAME: Floppy Disk Support

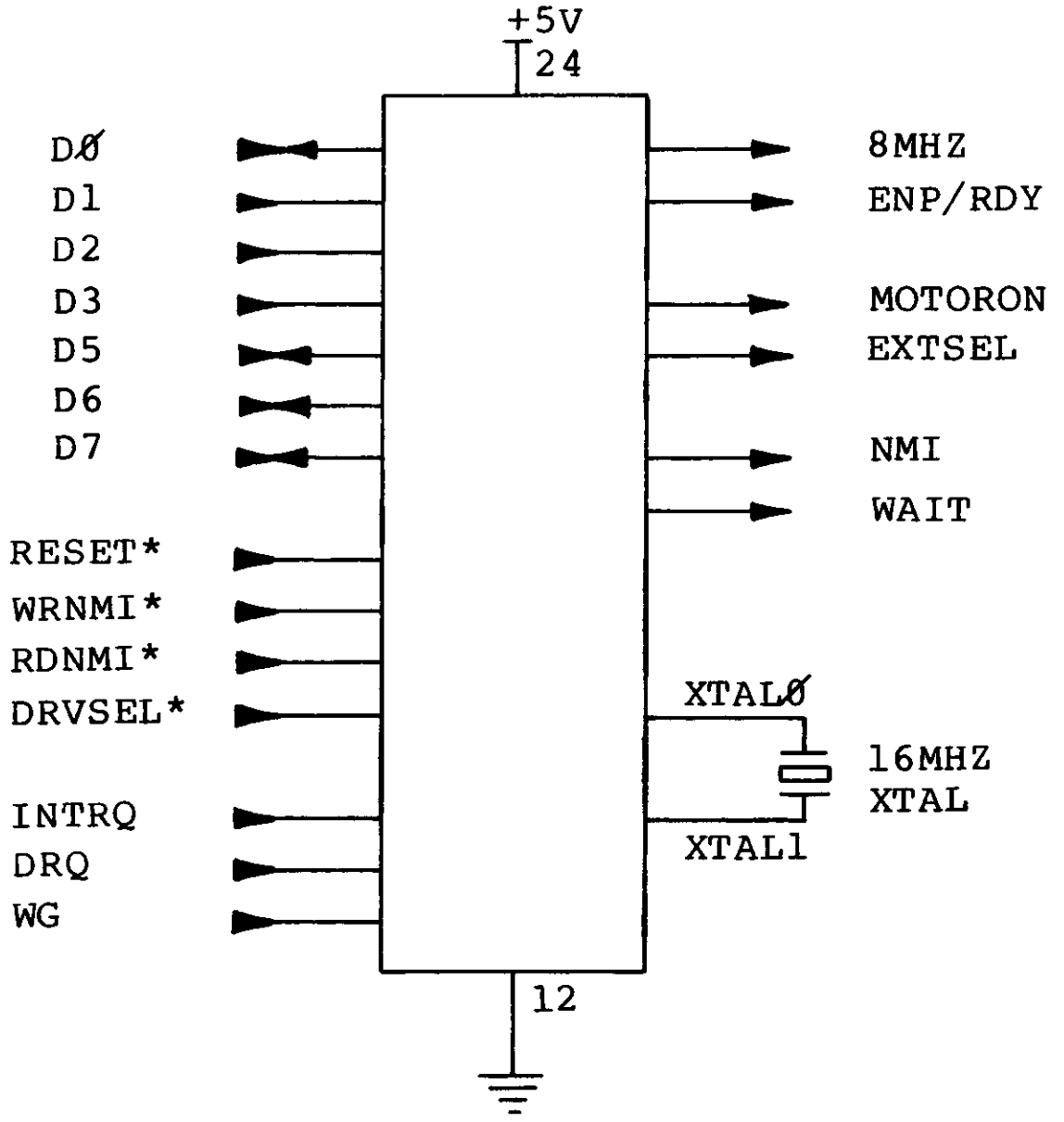
NO. OF PINS: 24

MAX. CLOCK FREQ.: 8 MHz

MAX. PROP. DELAY THROUGHPUT: 75 ns

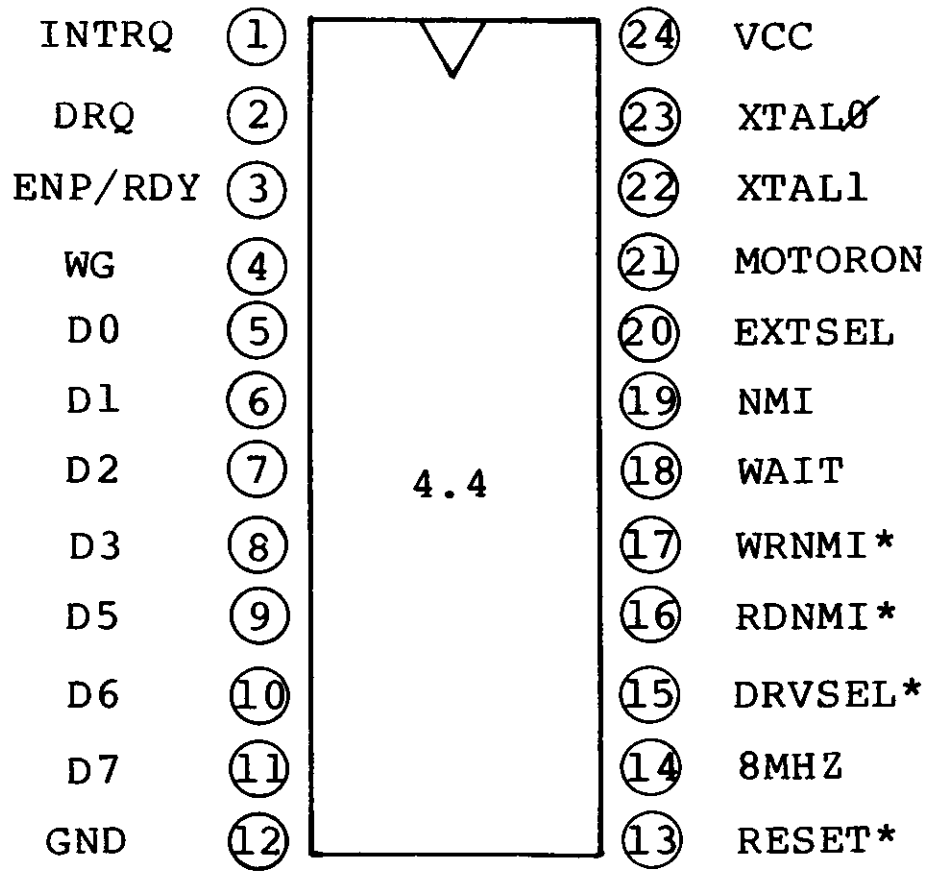
OPER. TEMP: Ø° C to 7Ø° C

OPERATING VOLTAGE & RANGE: 5 V ± 5%



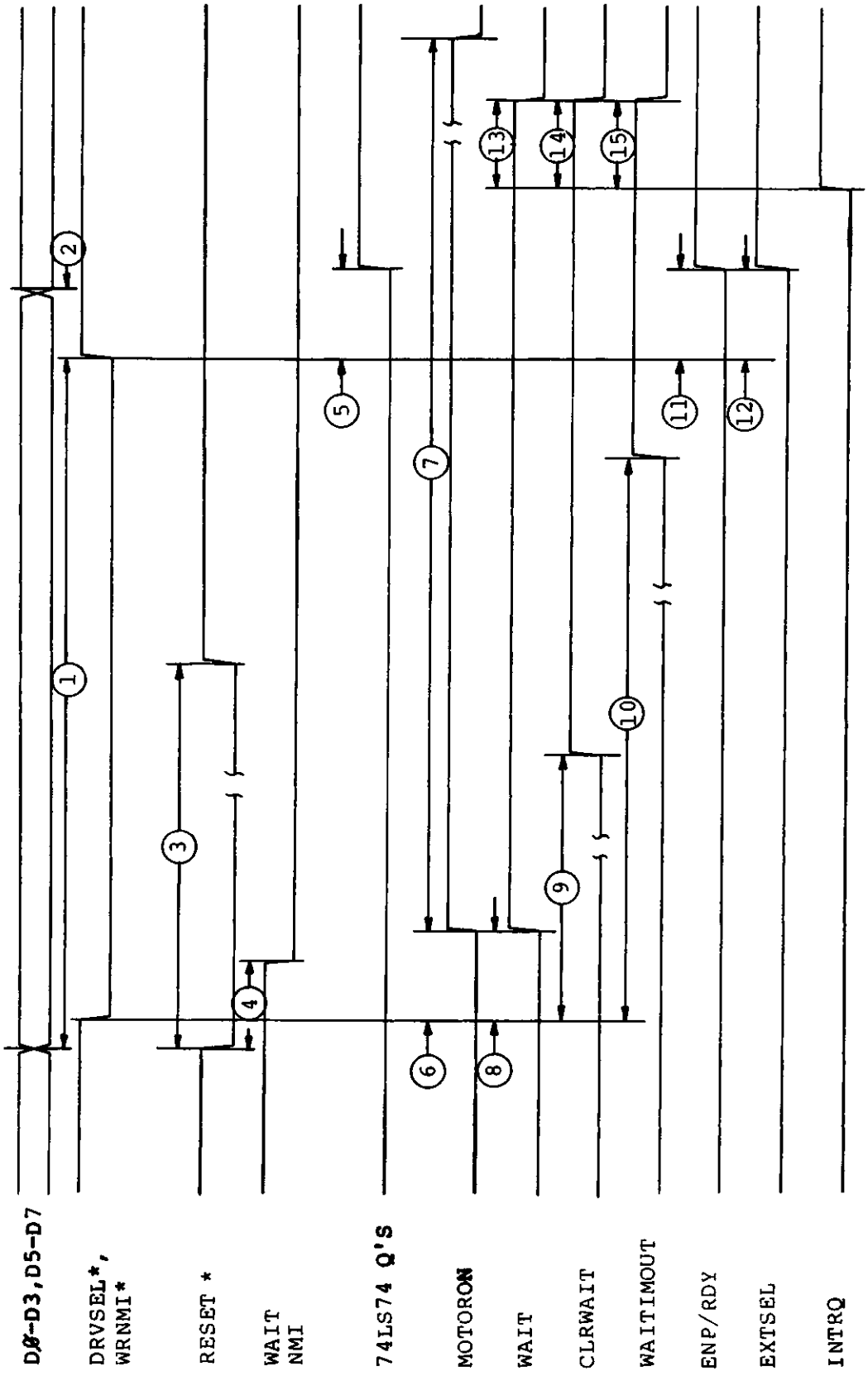
24 PIN CHIP

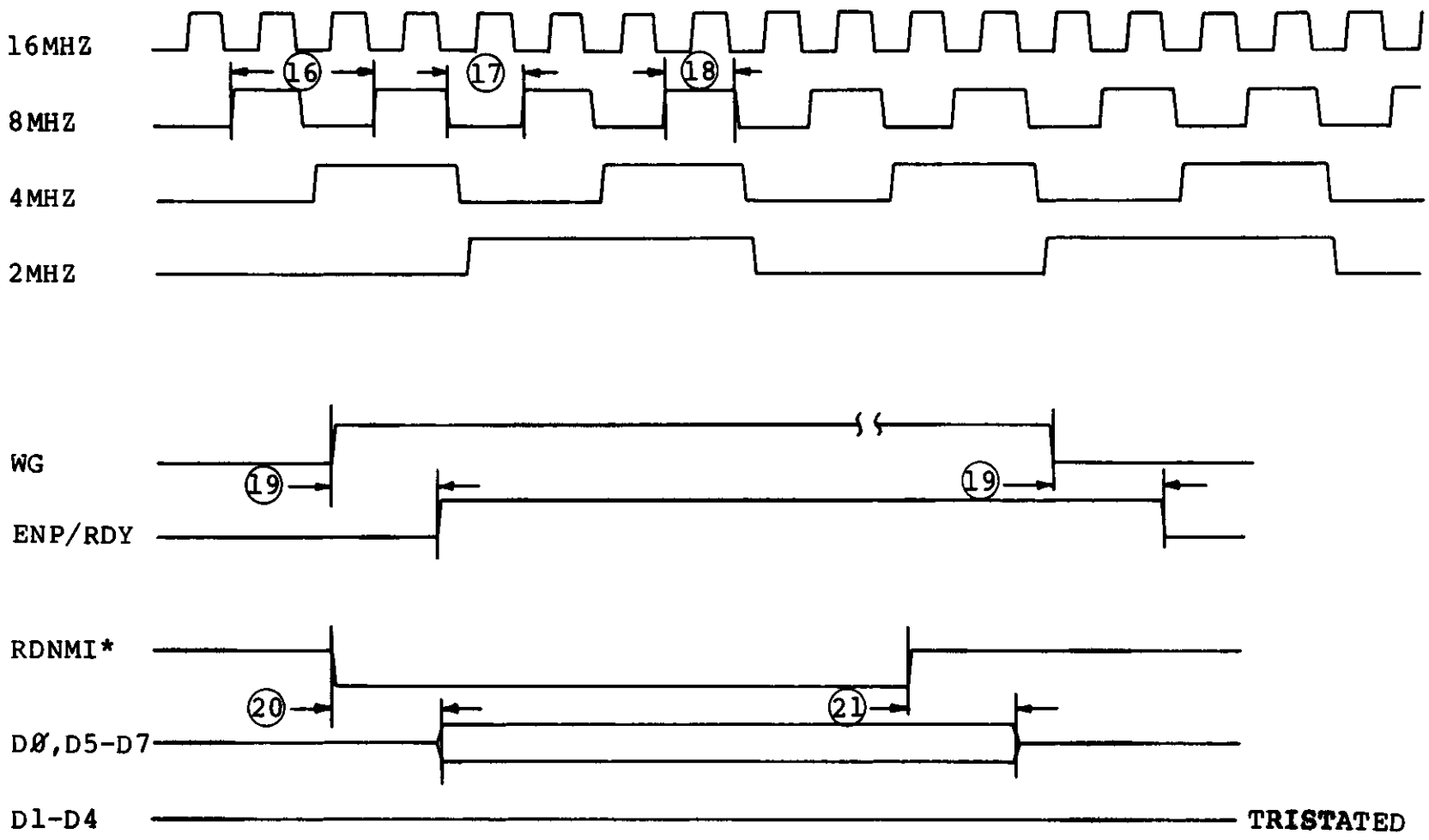
FLOPPY DISK SUPPORT


INTRQ 1
DRQ 2
ENP/RDY 3
WG 4
D0 5
D1 6
D2 7
D3 8
D5 9
D6 10
D7 11
GND 12
4.4
24 VCC
23 XTAL0
22 XTAL1
21 MOTORON
20 EXTSEL
19 NMI
18 WAIT
17 WRNMI*
16 RDNMI*
15 DRVSEL*
14 8MHZ
13 RESET*

	PARAMETER	MIN	SPEC. TYP	MAX	UNITS
1.	Data Setup Time	560			ns
2.	Data Hold Time	50			ns
3.	Reset* Pulse Width		70	100	µs
4.	Reset* ↓ to Wait or NMI ↓			75	ns
5.	WRNMI* ↑ to 74LS74 Q's Outputs ↓↑			75	ns
6.	DRVSEL* ↓ to MOTORON ↑			75	ns
*7.	MOTORON Pulse Width (Low)	3	4	5	sec.
8.	DRVSEL* ↓ to WAIT ↑			75	ns
9.	DRVSEL* ↓ to CLRWAIT ↑	500		1100	ns
10.	DRVSEL* ↓ to WAITIMOUT ↑	1024		1050	µs
11.	DRVSEL* ↑ to ENP/RDY ↑↓			75	ns
12.	DRVSEL* ↑ to EXTSEL ↑↓			75	ns
13.	INTRQ ↑ or DRQ ↑ to WAIT ↓			75	ns
14.	INTRQ ↑ or DRQ ↑ to CLRWAIT ↓			75	ns
15.	INTRQ ↑ or DRQ ↑ to WAITIMOUT ↓			75	ns
16.	8 MHZ Cycle Time		125		ns
17.	8 MHZ Pulse Width (Low)	50	62.5		ns
18.	8 MHZ Pulse Width (High)	50	62.5		ns
19.	WG ↑↓ to ENP/RDY ↑↓			75	ns
20.	RDNMI* ↓ to D0, D5-D7 Valid			75	ns
21.	RDMMI* ↑ to D0, D5-D7 Tristate 0			75	ns

* MOTORON Circuit Must Simulate a Retriggerable Monostable Multivibrator (74LS123)


D0-D3,D5-D7
DRVSEL*,
WRNMI*
RESET *
WAIT
NMI
74LS74 Q'S
MOTORON
WAIT
CLRWAIT
WAITIMOUT
ENP/RDY
EXTSEL
INTRQ
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15


16MHZ
8MHZ
4MHZ
2MHZ
16
17
18
WG
ENP/RDY
19
19
RDNMI*
DØ,D5-D7
20
21
D1-D4
TRISTATED

CAPACITANCE LOAD

OUTPUT	CAPACITANCE MAX.
DØ	8Ø pf
D5	8Ø pf
D6	8Ø pf
D7	8Ø pf
8 MHZ	15 pf
ENP/RDY	15 pf
MOTORON	15 pf
EXTSEL	15 pf
NMI	15 pf
WAIT	15 pf

DC CHARACTERISTICS 0° – 70° C

(ALL PINS)

PARAMETER	MIN.	TYP.	MAX.	UNITS
Input Voltage Level (High)	2.0			V
Input Voltage Level (Low)			.8	V
Output Voltage Level (High)	2.7	3.5		V
Output Voltage Level (Low)		.35	.5	V
(ALL PINS EXCEPT MOTORON & D0, D5-D7)				
Input Current Level (High)			20	μa
Input Current Level (Low)			–.4	ma
Output Current Level (High)	–160			μa
Output Current Level (Low)	3.2			ma
MOTORON				
Output Current Level (High)	–240			μa
Output Current Level (Low)	4.8			ma
D0, D5-D7				
Input Current Level (High)			20	μa
Input Current Level (Low)			–.4	ma
Output Current Level (High)	–280			μa
Output Current Level (Low)	5.6			ma

ARRAY #: 4.5.Ø

CIRCUIT NAME: RS232 Support

NO. OF PINS: 4Ø

OPER. TEMP.: Ø° C to 7Ø° C

OPER. VOLTAGE: 5V ± 5%


VCC
A0 1
A1 2
RDINTSTATUS 3
WRINTMASKREG 4
RS232IN 5
RS232OUT 6
CTS 14
DSR 15
CD 16
RI 20
RD 13
PE 26
FE 25
DE 24
THRE 22
DR 19
RTCIN 36
XINT 35
WR 39
N. C. 11
4.5.0
40 PIN
12
9 RTS
10 DTR
7 SRTS
8 ENTD
21 OUTE8
38 OUTE9
11 OUTEA
23 OUTEB
18 INEB
37 INT
27 BD0
28 BD1
29 BD2
30 BD3
31 BD4
32 BD5
33 BD6
34 BD7

D. C. CHARACTERISTICS 0° – 70° C

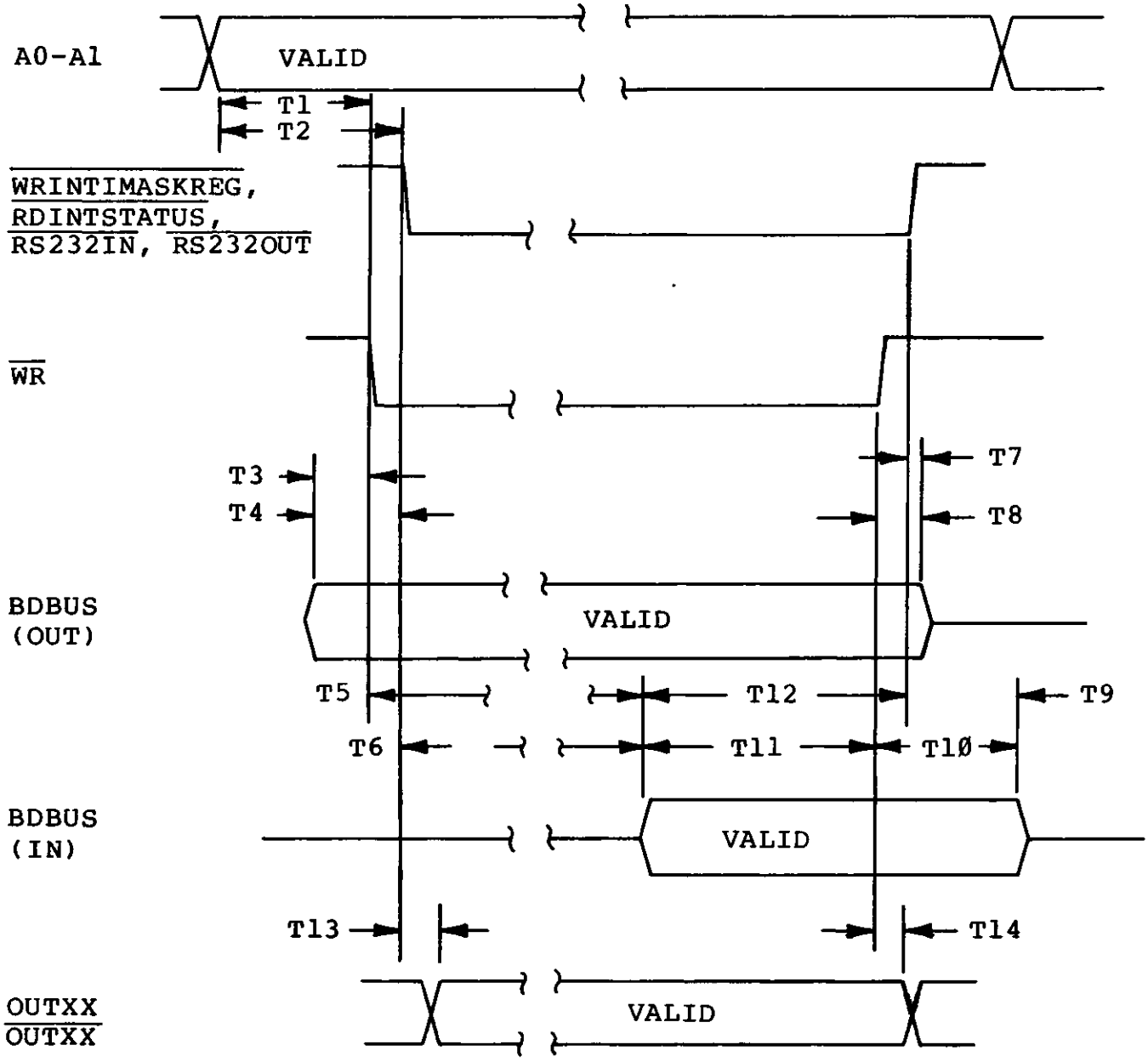
		MIN.	TYP.	MAX.	UNITS
Input Voltage (High)	V_{IH}	2.0			V
Input Voltage (Low)	V_{IL}			.8	V
Output Voltage (High)	V_{OH}	2.7	3.5		V
Output Voltage (Low)	V_{OL}		.35	.5	V
Input Current (High)	I_{IH}			20	μa
Input Current (Low)	I_{IL}			−.4	ma
Output Current (High)	I_{OH} (all except $\overline{INT}$, $\overline{INEB}$ & BD)	120			μa
	$\overline{INT}$ (O.C. or D.D.)	120			μa
	BD BUS	280			μa
	$\overline{INEB}$	120			μa
Output Current (Low)	**I_{OL} (all except $\overline{INT}$, $\overline{INEB}$, & BD)**	−3.2			ma
	$\overline{INT}$, (O. C. or D.D.)	−8.0			ma
	BD BUS	−5.6			ma
	$\overline{INEB}$	−4.4			ma

PROP, DELAY & TIMING	MIN.	TYP.	MAX.
Data In* to BD Bus			75
$\overline{\text{RS232 IN}}$ ↓ to BD Bus			75
BD Bus Set Up to $\overline{\text{WR}}$ ↑	75		
BD Bus Hold Time From $\overline{\text{WR}}$ ↑			60
AØ, A1 to $\overline{\text{INEB}}$, OUTEB, OUTE9, OUTEA, $\overline{\text{OUTEB}}$			75
$\overline{\text{RS232IN}}$, $\overline{\text{RS232OUT}}$ ↓ to $\overline{\text{INEB}}$ OUTE8, OUTE9, OUTEA, $\overline{\text{OUTEB}}$			75
$\overline{\text{WR}}$ ↑ to OUTE8, OUTE9, OUTEA, $\overline{\text{OUTEB}}$ (WOULD LIKE 18)			32
$\overline{\text{RS232OUT}}$ ↓ to $\overline{\text{RTS}}$, $\overline{\text{DTR}}$, ENTD, $\overline{\text{SRTS}}$			75
PE, FE, DE, THRE, DR, RTCIN, XINT to $\overline{\text{INT}}$ ↓			75

All Delay In NSEC.

*Data in is **any** of the following inputs: PE, FE, DE, THRE, DR, RTCIN, XINT, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{CD}}$, $\overline{\text{RI}}$ & $\overline{\text{RD}}$.

C_{OUT} Max = 100 pf for BD Bus, $\overline{\text{INT}}$, & $\overline{\text{INEB}}$; all others C_{OUT} Max = 50 pf.


A0-A1
VALID
T1
T2
WRINTIMASKREG,
RDINTSTATUS,
RS232IN, RS232OUT
WR
T3
T4
T7
T8
BDBUS
(OUT)
VALID
T5
T12
T9
T6
T11
T10
BDBUS
(IN)
VALID
T13
T14
OUTXX
OUTXX
VALID

	MIN.	TYP.	MAX.
t_1	168		
t_2	168		
t_3	−34		Ø
t_4	−34		Ø
t_5			75
t_6			75
t_7			34
t_8			6Ø
t_9	24		25Ø
t_{10}	24		25Ø
t_{11}	75		
t_{12}	75		
t_{13}			75
t_{14}			32

(Need 18)

All Timing in NSEC.

Index

Index

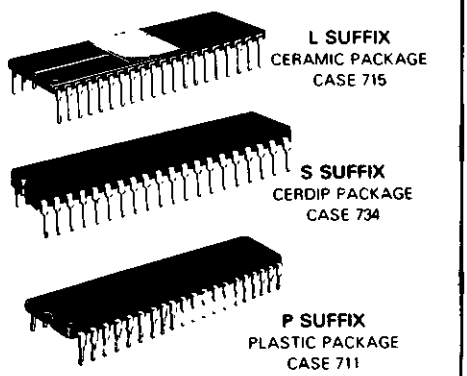
MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC6835

Advance Information

MOS
(HIGH-DENSITY, N-CHANNEL, SILICON-GATE DEPLETION LOAD)

MASK PROGRAMMED CRT CONTROLLER (CRTC)



L SUFFIX
CERAMIC PACKAGE
CASE 715

S SUFFIX
CERDIP PACKAGE
CASE 734

P SUFFIX
PLASTIC PACKAGE
CASE 711

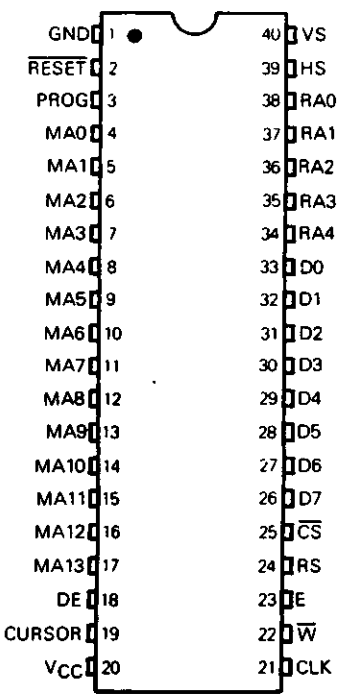
CRT CONTROLLER (CRTC)

The MC6835 is a ROM based CRT Controller which interfaces an MPU system to a raster scan CRT display. It is intended for use in MPU based controllers for CRT terminals in stand-alone or cluster configurations. The MC6835 supports two selectable mask programmed screen formats using the program select input (PROG).

The CRTC is optimized for the hardware/software balance required for maximum flexibility. All keyboard functions, reads, writes, cursor movements, scrolling, and editing are under processor control. The mask programmed registers of the CRTC are programmed to control the video format and timing.

- Cost Effective ROM Based CRTC Which Supports Two Screen Formats
- Useful in Monochrome or Color CRT Applications
- Applications Include "Glass-Teletype," Smart, Programmable, Intelligent CRT Terminals; Video Games; Information Displays
- Alphanumeric, Semigraphic, and Full Graphic Capability
- Timing May Be Generated for Almost Any Alphanumeric Screen Format, e.g., 80 × 24, 72 × 64, 132 × 20
- Single +5 Volt Supply
- M6800 Compatible Bus Interface
- TTL-Compatible Inputs and Outputs
- Start Address Register Provides Hardware Scroll (By Page, Line, or Character)
- Programmable Cursor Register Allows Control of Cursor Position
- Refresh (Screen) Memory May Be Multiplexed Between the CRTC and the MPU Thus Removing the Requirements for Line Buffers or External DMA Devices
- Mask Programmable Interlace or Non-Interlace Scan Modes
- 14-Bit Refresh Address Allows Up to 16K of Refresh Memory for Use in Character or Semigraphic Displays
- 5-Bit Row Address Allows up to 32 Scan-Line Character Blocks
- By Utilizing Both the Refresh Addresses and the Row Addresses, a 512K Address Space is Available for Use in Graphics Systems
- Refresh Addresses are Provided During Retrace, Allowing the CRTC to provide Row Addresses to Refresh Dynamic RAMs
- Pin Compatible with the MC6845. The MC6845 May Be Used as a Prototype Part to Emulate the MC6835.

PIN ASSIGNMENT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}*	−0.3 to +7.0	V
Input Voltage	V_{in}*	−0.3 to +7.0	V
Operating Temperature Range MC6835, MC68A35, MC68B35 MC6835C, MC68A35C, MC68B35C	T_A	0 to +70 −50 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

*With respect to GND (V_{SS}).

This document contains information on a new product. Specifications and information herein are subject to change without notice

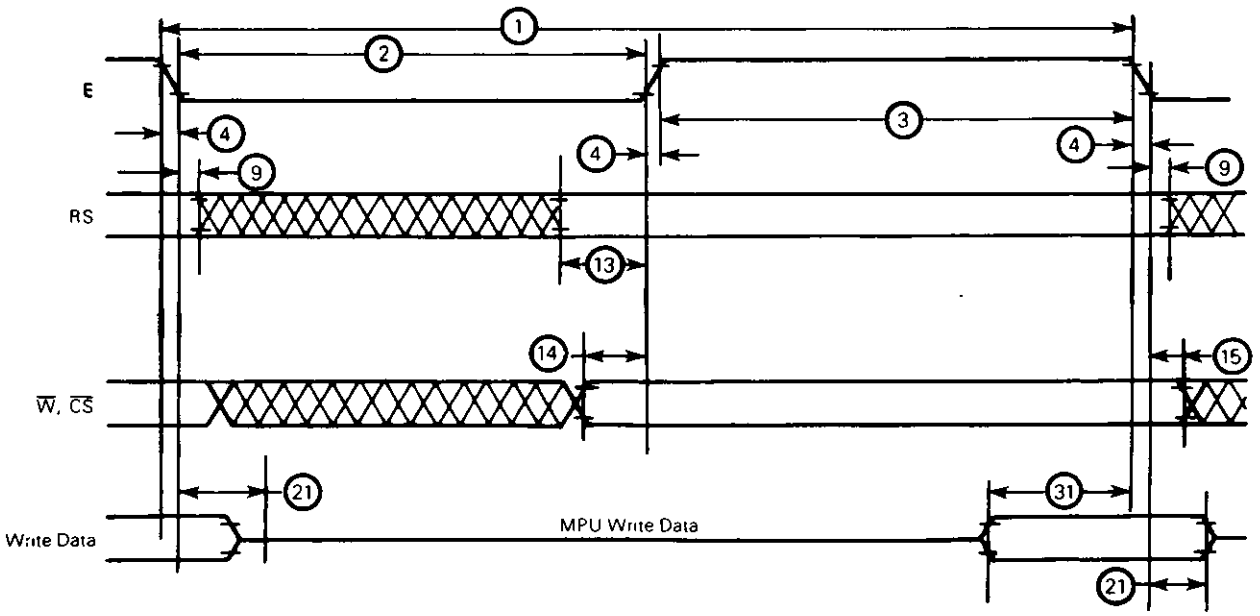
DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted) (Reference Figures 2,4)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage		V_{IL}	-0.3	–	0.8	V
Input Leakage Current		I_{in}	–	0.1	2.5	μA
Hi Z (Off State) Input Current (V_{CC} = 5.25 V) (V_{in} = 0.4 to 2.4 V)		I_{TSI}	-10	–	10	μA
Output High Voltage (I_{Load} = – 100 μA)			2.4	3.0	–	V
Output Low Voltage (I_{load} = 1.6 mA)		V_{OL}	–	0.3	0.4	V
Internal Power Dissipation (Measured at T_A = 0°C)		P_D	–	150	300	mW
Input Capacitance	D0-D7	C_{in}	–	–	12.5	pF
	All Others		–	–	10	
Output Capacitance	All Outputs	C_{out}	–	–	10	pF

BUS TIMING CHARACTERISTICS (Reference Figures 2 and 3)

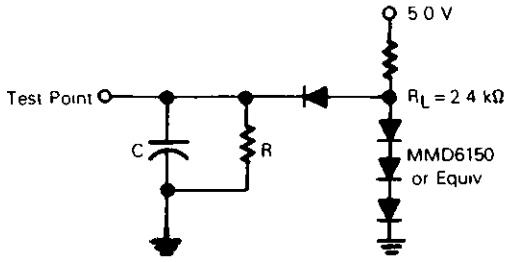
Ident Number	Characteristics	Symbol	MC6835		MC68A35		MC68B35		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	–	280	–	210	–	ns
3	Pulse Width, E High	PW_{EH}	450	–	280	–	220	–	ns
4	Clock Transition Time	t_r, t_f	–	25	-	25	–	20	ns
9	Address Hold Time (RS)	t_{AH}	10	–	10	–	10	–	ns
13	RS Setup Before E	t_{AS}	80	–	60	–	40		ns
14	$\overline{W}$ and $\overline{CS}$ Setup Before E	t_{CS}	80	–	60	–	40	–	ns
15	Hold Time for $\overline{W}$ and $\overline{CS}$	t_{CH}	10	–	10	–	10	–	ns
21	Write Data Hold Time Required	t_{DHW}	10	–	10	–	10	–	ns
31	Peripheral Input Data Setup	t_{DSW}	165	–	80	–	60	–	ns

FIGURE 2 – MC6835 BUS TIMING



NOTES
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V unless otherwise noted
2. Measurement points shown are 0.8 V and 2.0 V unless otherwise noted

FIGURE 3 — BUS TIMING TEST LOAD

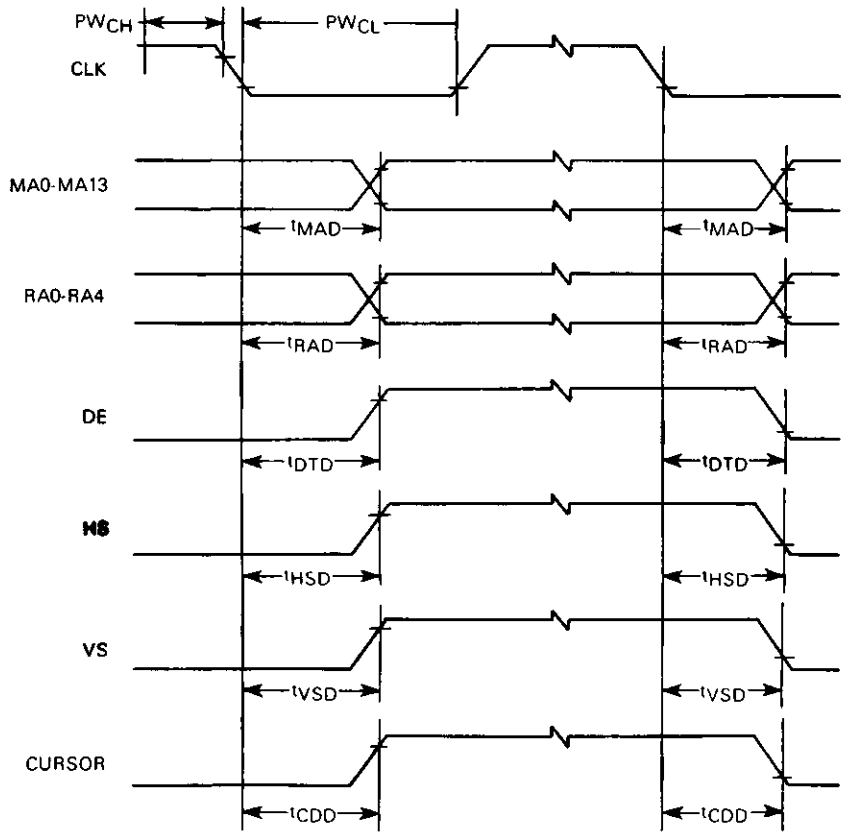


C = 130 pF for D0-D7
= 30 pF for MA0-MA13, RA0-RA4, DE, HS, VS, and CURSOR
R = 11 kΩ for D0-D7
= 24 kΩ for All Other Outputs

CRTC TIMING CHARACTERISTICS (See Figure 4)

Characteristics	Symbol	MC6835		MC68A35		MC68B35		Unit
		Min	Max	Min	Max	Min	Max	
Minimum Clock Pulse Width, Low	PW_{CL}	150	–	140	–	130	–	ns
Minimum Clock Pulse Width, High	PW_{CH}	150	–	140	–	130	–	ns
Clock Frequency	f_c	330	–	300	–	270	–	ns
Rise and Fall Time for Clock Input	t_r, t_f	–	20	–	20	–	20	ns
Memory Address Delay Time	t_{MAD}	–	160	–	160	–	160	ns
Raster Address Delay Time	t_{RAD}	–	160	–	160	–	160	ns
Display Timing Delay Time	t_{DTD}	–	250	–	250	–	200	ns
Horizontal Sync Delay Time	t_{HSD}	–	250	–	250	–	200	ns
Vertical Sync Delay Time	t_{VSP}	–	250	–	250	–	200	ns
Cursor Display Timing Delay Time	t_{CDD}	–	250	–	250	–	200	ns

FIGURE 4 — CRTC TIMING CHART



NOTE Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise noted

CRTC INTERFACE SYSTEM DESCRIPTION

The MC6835 CRT Controller generates the signals necessary to interface a digital system to a raster scan CRT display In this type of display, an electron beam starts in the upper left hand corner, moves quickly across the screen and returns This action is called a horizontal scan After each horizontal scan the beam is incrementally moved down in the vertical direction until it has reached the bottom At this point one frame has been displayed, as the beam has made many horizontal scans and one vertical scan

Two types of raster scanning are used in CRTs, interlace and non-interlace, shown in Figures 5 and 6 Non-interlacing scanning consists of one field per frame The scan lines in Figure 5 are shown as solid lines and the retrace patterns are indicated by the dotted lines Increasing the number of frames per second will decrease the flicker Ordinarily, either a 50 or 60 frame per second refresh rate is used to minimize beating between the frequency of the CRT horizontal oscillator and the power line frequency This prevents the displayed data from weaving or swimming

Interlace scanning is used in broadcast TV and on data monitors where high density or high resolution data must be displayed Two fields, or vertical scans are made down the screen for each single picture or frame The first field (Even field) starts in the upper left hand corner, the second (Odd field) in the upper center Both fields overlap as shown in Figure 6, thus interlacing the two fields into a single frame

In order to display the characters on the CRT screen the frames must be continually repeated The data to be displayed is stored in the Refresh (Screen) memory by the MPU controlling the data processing system The data is usually written in ASCII code, so it cannot be directly displayed as characters A Character Generator ROM is typically used to convert the ASCII codes into the "dot" pattern for every character

The most common method of generating characters is to create a matrix of "x" dots (columns) wide and "y" dots (rows) high Each character is created by selectively filling in the dots As "x" and "y" get larger a more detailed character may be created Two common dot matrices are 5 x 7 and 7 x 9 Many variations of these standards will allow Chinese, Japanese, or Arabic letters instead of English Since characters require some space between them, a character block larger than the character is typically used as shown in Figure 7 The figure also shows the corresponding timing and levels for a video signal that would generate the characters

FIGURE 5 — RASTER SCAN SYSTEM (NON-INTERLACE)

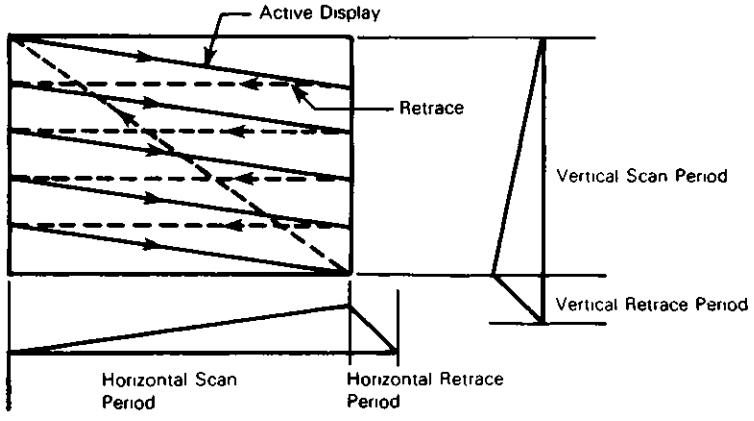


FIGURE 6 — RASTER SCAN SYSTEM (INTERLACE)

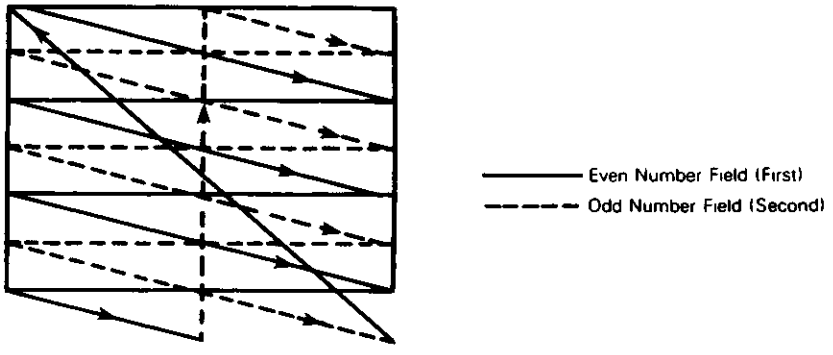
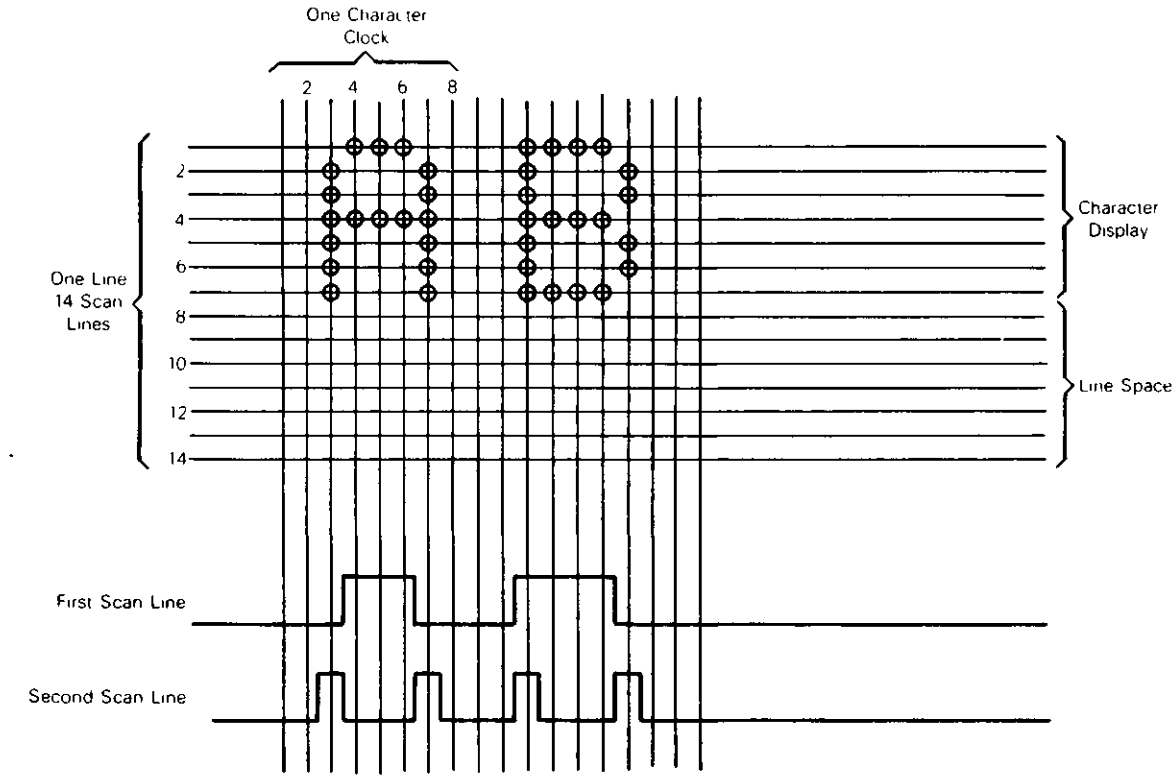


FIGURE 7 — CHARACTER DISPLAY ON THE SCREEN AND VIDEO SIGNAL



Referring to Figure 1, the MC6835 CRT controller generates the Refresh addresses (MA0-MA13), row addresses (RA0-RA4), and the video timing (vertical sync — VS, horizontal sync — HS and display enable — DE) Other functions include an internal cursor register which generates a Cursor output when its contents compare to the current Refresh address A select input, PROG, allows selection of one of two mask programmed video formats (e g , for 50 Hz and 60 Hz compatibility)

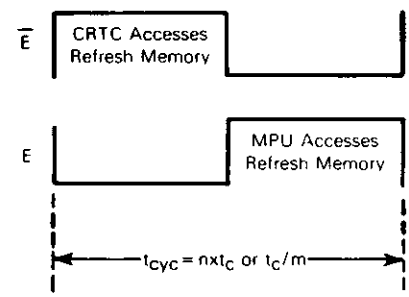
All timing in the CRTC is derived from the CLK input In alphanumeric terminals, this signal is the character rate The video rate or "dot" clock is externally divided by high speed logic (TTL) to generate the CLK signal The high speed logic must also generate the timing and control signals necessary for the Shift Register, Latch and MUX Control shown in Figure 1

The processor communicates with the CRTC through an 8-bit data bus by writing into the five user programmable registers of the MC6835

The Refresh memory address is multiplexed between the processor and the CRTC Data appears on a secondary bus separate from the processor's bus The secondary data bus concept in no way precludes using the Refresh RAM for other purposes It looks like any other RAM to the processor A number of approaches are possible for solving contentions for the Refresh memory

1 Processor always gets priority (Generally, "hash" occurs as MPU and CRTC clocks are not synchronized)
2 Processor gets priority access anytime, but can be synchronized by an interrupt to perform accesses only during horizontal and vertical retrace times
3 Synchronize the processor with memory wait cycles (states)
4 Synchronize the processor to the character rate as shown in Figure 8 The M6800 processor family works very well in this configuration as constant cycle lengths are present This method provides no overhead for the processor as there is never a contention for a memory access All accesses are transparent

FIGURE 8 — TRANSPARENT REFRESH MEMORY CONFIGURATION TIMING USING M6800 FAMILY MPU



Where m, n are integers, t_C is character period

PIN DESCRIPTION

PROCESSOR INTERFACE

The CRTC interfaces to a processor bus on the data bus (D0-D7) using $\overline{CS}$, RS, E, and $\overline{W}$ for control signals

Data Bus (D0-D7) – The data lines (D0 D7) comprise the write only data bus

Enable (E) – The Enable signal is a high-impedance TTL/MOS-compatible input which enables the data bus input/output buffers and clocks data to the CRTC This signal is usually derived from the processor clock The high to low transition is the active edge

Chip Select ($\overline{CS}$) – The $\overline{CS}$ line is an active-low high-impedance TTL/MOS-compatible input which selects the CRTC write to the internal register file This signal should only be active when there is a valid stable address being decoded from the processor

Register Select (RS) – The RS line is a high-impedance TTL/MOS-compatible input which selects either the Address Register (RS = "0") or one of the Data Registers (RS = "1") of the internal register file when $\overline{CS}$ is low

Write ($\overline{W}$) – The $\overline{W}$ line is a high-impedance TTL/MOS-compatible input which determines whether the internal register file gets written A write is defined as a low level

CRT CONTROL

The CRTC provides horizontal sync (HS), vertical sync (VS), and display enable (DE) signals

NOTE – Care should be exercised when interfacing to CRT monitors as many monitors claiming to be "TTL compatible," have transistor input circuits which require the CRTC or TTL devices buffering signals from the CRTC/video circuits to exceed the maximum rated drive currents

Vertical Sync (VS) and Horizontal Sync (HS) – These TTL-compatible outputs are active-high signals which drive the monitor directly or are fed to the video processing circuitry to generate a composite video signal The VS signal determines the vertical position of the displayed text while the HS signal determines the horizontal position of the displayed text

Display Enable (DE) – This TTL-compatible output is an active-high signal which indicates the CRTC is providing addressing in the active Display Area

REFRESH MEMORY/CHARACTER GENERATOR ADDRESSING

The CRTC provides Memory Addresses (MA0-MA13) to scan the Refresh RAM Row Addresses (RA0-RA4) are also provided for use with character generator ROMs In a graphics system both the Memory Addresses and the Row Addresses would be used to scan the Refresh RAM Both the Memory Addresses and the Row Addresses continue to run during vertical retrace thus allowing the CRTC to provide the refresh addresses required to refresh dynamic RAMs

Refresh Memory Addresses (MA0-MA13) – These 14 outputs are used to refresh the CRT screen with pages of data located within a 16K block of refresh memory These outputs are capable of driving one standard TTL load and 30 pF

Row Addresses (RA0-RA4) – These five outputs from the internal Row Address counter are used to address the Character Generator ROM These outputs are capable of driving one standard TTL load and 30 pF

OTHER PINS

Cursor – This TTL-compatible output indicates a valid Cursor address to external video processing logic It is an active-high signal

Clock (CLK) – The CLK is a TTL/MOS-compatible input used to synchronize all CRT functions except for the processor interface An external dot counter is used to derive this signal which is usually the character rate in an alphanumeric CRT The active transition is high-to-low

Program Select (PROG) – This TTL-compatible input allows selection of one of two sets of mask programmed video formats Set zero is selected when PROG is low and set one is selected when PROG is high

V_{CC}, GND – These inputs supply +5 Vdc ±5% to the CRTC

$\overline{RESET}$ – The $\overline{RESET}$ input is used to reset the CRTC Functionality of $\overline{RESET}$ differs from that of other M6800 parts $\overline{RESET}$ must remain low for at least one cycle of the character clock (CLK) A low level on the $\overline{RESET}$ input forces the CRTC into the following state

a All counters in the CRTC are cleared and the device stops the display operation
b All the outputs are driven low, except the MA0-MA13 outputs which are driven to the current value in the Start Address Register
c The control registers of the CRTC are not affected and remain unchanged
d The CRTC resumes the display operation immediately after the release of $\overline{RESET}$

CRTC DESCRIPTION

The CRTC consists of mask-programmable horizontal and vertical timing generators, software-programmable linear address register, mask-programmable cursor logic and control circuitry for interfacing to a M6800 family microprocessor bus

All CRTC timing is derived from CLK, usually the output of an external dot rate counter Coincidence (CO) circuits continuously compare counter contents to the contents of the

TABLE 1 — INTERNAL REGISTER ASSIGNMENT

CS	RS	Address Register 4	3	2	1	0	Register #	Register File	Program Unit	Read	Write	Number of Bits 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	–	–	–	–								
0	0	X	X	X	X	X	AR	Address Register	–	No	Yes								
							R0	Horizontal Total	Char	No	No								
							R1	Horizontal Displayed	Char	No	No								
							R2	H Sync Position	Char	No	No								
							R3	Sync Width	–	No	No	V	V	V	V	H	H	H	H
							R4	Vertical Total	Char Row	No	No								
							R5	V Total Adjust	Scan Line	No	No								
							R6	Vertical Displayed	Char Row	No	No								
							R7	V Sync Position	Char Row	No	No								
							R8	Interlace Mode and Skew	Note 1	No	No	C	C	D	D			I	I
							R9	Max Scan Line Address	Scan Line	No	No								
							R10	Cursor Start	Scan Line	No	No		B	P			(Note 2)		
							R11	Cursor End	Scan Line	No	No								
0	1	0	1	1	0	0	R12	Start Address (H)	–	No	Yes	0	0						
0	1	0	1	1	0	1	R13	Start Address (L)	–	No	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	–	No	Yes	0	0						
0	1	0	1	1	1	1	R15	Cursor (L)	–	No	Yes								

Note 3

NOTES
1 The Interlace Control is shown in Table 2 while Skew Control is shown in Table 3
2 Bit 5 of the Cursor Start Raster Register is used to blink period control, and Bit 6 is used to select blink or non-blink
3 R0-R11 are mask-programmable and are not accessible via the data bus

mask programmable register file, R0-R11 For horizontal timing generation, comparisons result in

1 Horizontal sync pulse (HS) of a frequency, position and width determined by the register contents
2 Horizontal Display signal of a frequency, position and duration determined by the register contents

The horizontal counter produces H clock which drives the Scan Line Counter and Vertical Control The contents of the Raster Counter are continuously compared to the Max Scan Line Address Register A coincidence resets the Raster Counter and clocks the Vertical Counter

Comparisons of Vertical Counter contents and Vertical Registers result in

1 Vertical sync pulse (VS) of a frequency, position and width determined by the register contents
2 Vertical Display signal of a frequency, position, and duration determined by the register contents

The Vertical Control Logic has other functions

1 Generate row selects, RA0-RA4, from the Raster Count for the corresponding interlace or non-interlace modes
2 Extend the number of scan lines in the vertical total by the amount programmed in the Vertical Total Adjust Register

The cursor logic determines the size and blink rate of the cursor as indicated by the register contents

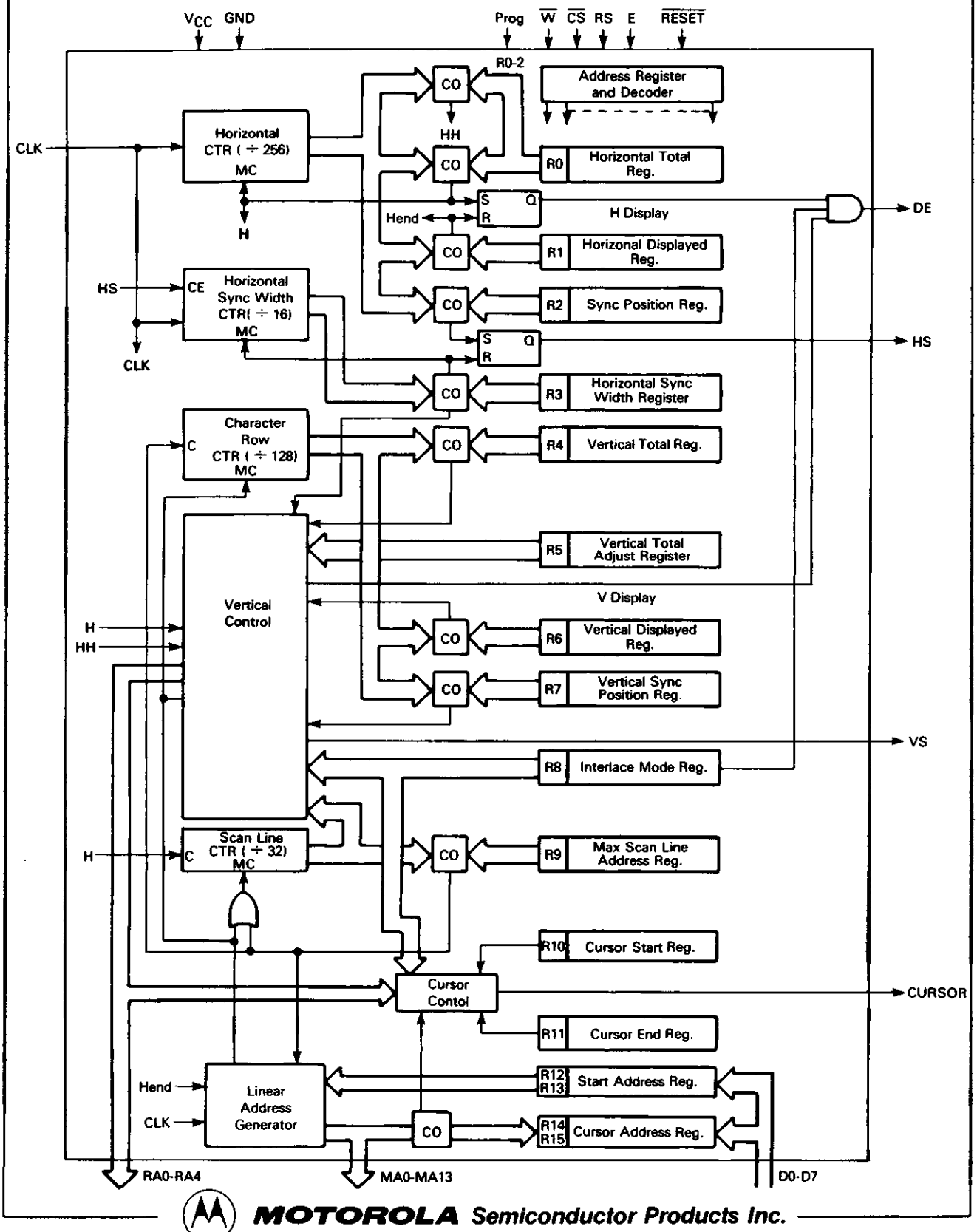
The Linear Address Generator is driven by CLK and locates the relative positions of characters in memory and their positions on the screen Fourteen outputs, MA0-MA13, are available for addressing up to four pages of 4K characters, eight pages of 2K characters, etc

Five additional write-only registers define the Start Address and cursor position Using the Start Address Register, hardware scrolling through 16K characters is possible The Linear Address Generator repeats the same sequence of addresses for each scan line of a character row The Start Address Register and the Cursor Position Register are programmed by the processor through the data bus, D0-D7 and the control signals — $\overline{W}$, $\overline{CS}$, RS, and E Refer to Figure 9

REGISTER FILE DESCRIPTION

The MC6835 has 17 control registers of which 12 are mask programmable The remaining five registers — Address register, Start Address register pair, and Cursor Position register pair — are write-only registers programmed by the MPU These registers control horizontal timing, vertical timing, interlace operation, row address operation and define the cursor, cursor address, and start address The register addresses and sizes are shown in Table 1

FIGURE 9 – CRTC BLOCK DIAGRAM



MASK PROGRAMMABLE REGISTERS R0-R11

The twelve mask programmable registers determine the display format generated by the MC6835 The PROG input is used to select one of two sets of register values

Figure 10 shows the visible display area of a typical CRT monitor giving the point of reference for horizontal registers as the left most displayed character position Horizontal registers are programmed in character clock time units with respect to the reference as shown in Figure 11 The point of reference for the vertical registers is the top character position displayed Vertical registers are programmed in character row times or scan line times as shown in Figure 12

Horizontal Total Register (R0) – This 8-bit register determines the horizontal sync (HS) frequency by defining the HS period in character times It is the total of the displayed characters plus the non-displayed character times (retrace) minus one

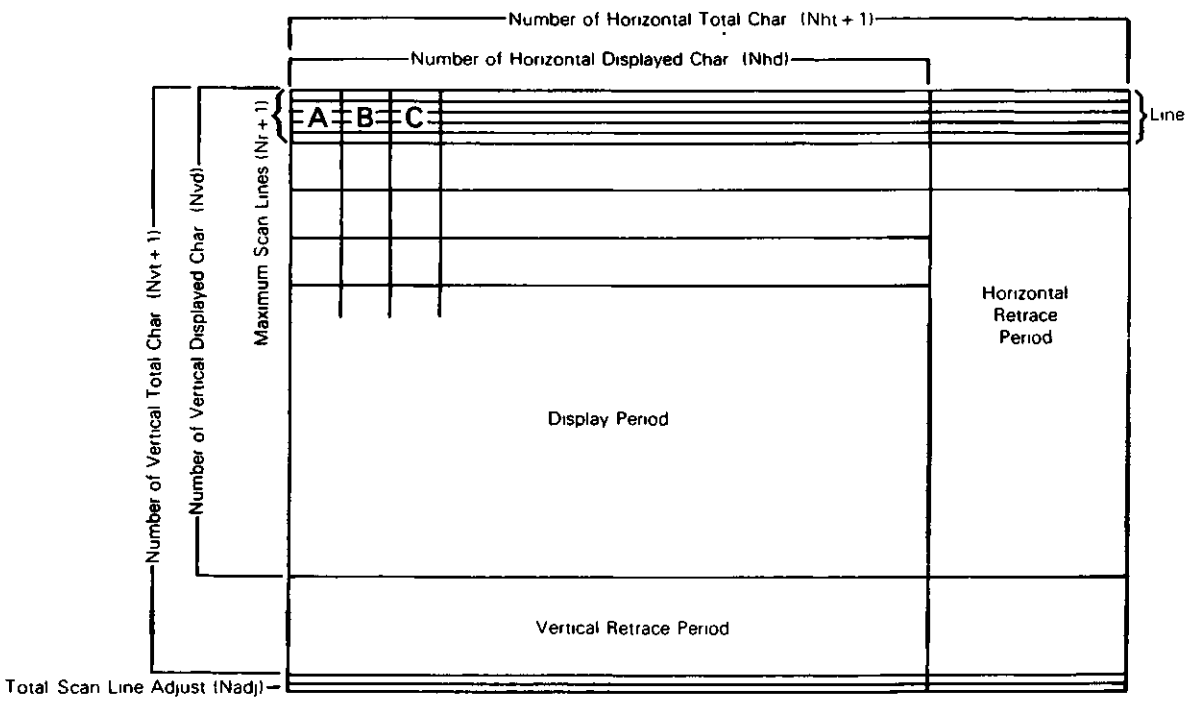
Horizontal Displayed Register (R1) – This 8-bit register determines the number of displayed characters per line Any 8-bit number may be programmed as long as the contents of R0 are greater than the contents of R1

Horizontal Sync Position Register (R2) – This 8-bit register controls the HS position The horizontal sync position defines the horizontal sync delay (Front Porch) and the horizontal scan delay (Back Porch) When the programmed value of this register is increased, the display on the CRT screen is shifted to the left When the programmed value is decreased the display is shifted to the right Any 8-bit number may be programmed as long as the sum of the contents of R1, R2, and the lower four bits of R3 are less than the contents of R0

Sync Width Register (R3) – This 8-bit register determines the width of the vertical sync (VS) pulse and the horizontal sync (HS) pulse Programming the upper four bits for 1-to-15 will select VS pulse widths from 1-to-15 scan-line times Programming the upper four bits as zeros will select a VS pulse width of 16 scan line times The HS pulse width may be programmed from 1-to-15 character clock periods thus allowing compatibility with the HS pulse width specifications of many different monitors If zeros are written into the lower four bits of this register, then no HS is provided

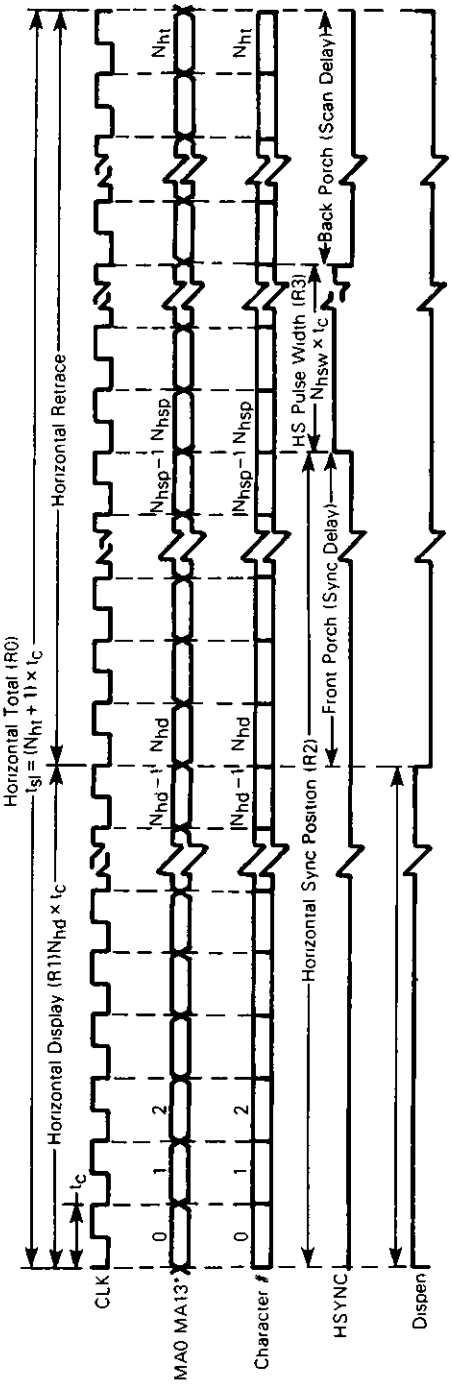
Horizontal Timing Summary (Figure 11) – The difference between R0 and R1 is the horizontal blanking interval This interval in the horizontal scan period allows the beam to return (retrace) to the left side of the screen The retrace time is determined by the monitor's horizontal scan components Retrace time is less than the horizontal blanking interval A good rule of thumb is to make the horizontal blanking about 20% of the total horizontal scanning period for a CRT In inexpensive TV receivers, the beam overscans the display screen so that aging of parts does not result in underscanning Because of this, the retrace time should be about 1/3 the horizontal scanning period The horizontal sync delay, HS pulse width and horizontal scan delay are typically programmed with 1 2 2 ratio

FIGURE 10 – ILLUSTRATION OF THE CRT SCREEN FORMAT



NOTE 1 Timing values are described in Table 8

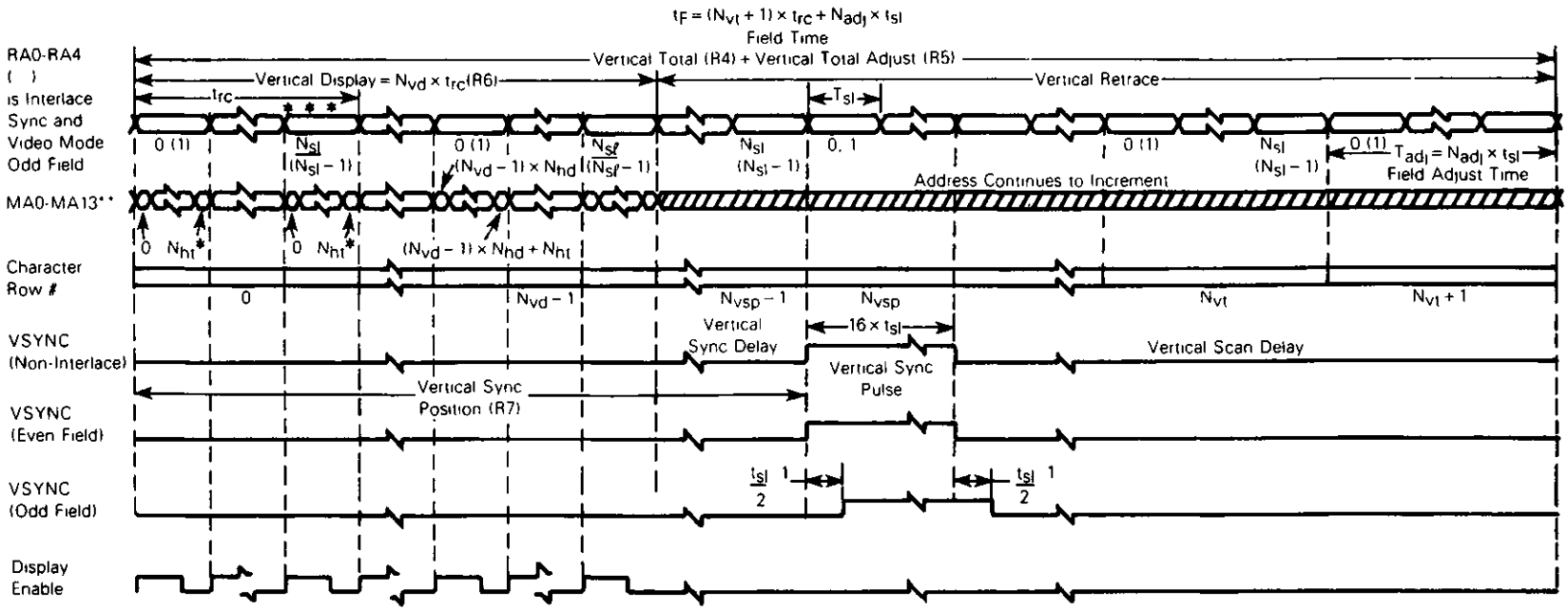
FIGURE 11 – CRTC HORIZONTAL TIMING



* Timing is shown for first displayed scan row only See Chart in Figure 15 for other rows The initial MA is determined by the contents of Start Address Register, R12/R13 Timing is shown for R12/R13=0

NOTE 1 Timing values are described in Table 5

FIGURE 12 — CRTC VERTICAL TIMING



*N_{ht} must be an odd number for both interlace modes.
**Initial MA is determined by R12/R13 (Start Address Register), which is zero in this timing example.
***N_{sl} must be an odd number for Interlace Sync and Video Mode

NOTES
1. Refer to Figure 6 — The Odd Field is offset ½ horizontal scan time.
2. Timing values are described in Table 5.

TABLE 4 — CURSOR AND DE SKEW CONTROL

Value	Skew
00	No Character Skew
01	One Character Skew
10	Two Character Skew
11	Not Available

Maximum Scan Line Address Register (R9) — This 5-bit register determines the number of scan lines per character row including the spacing thus controlling operation of the Row Address counter The programmed value is a maximum address and is one less than the number of scan lines

Cursor Start Register (R10) and Cursor End Register (R11) These registers allow a cursor of up to 32 scan lines in height to be placed on any scan line of the character block as shown in Figure 14 R10 is a 7 bit register used to define the start scan line and blink rate for the cursor Bits 5 and 6 of the Cursor Start Address Register control the cursor operation as shown in Table 4 Non-display, display and two blink modes (16 times or 32 times the field period) are available R11 is a 5-bit register which defines the last scan line of the cursor

When an external blink feature on characters is required, it may be necessary to perform cursor blink externally so that both blink rates are synchronized Note that an invert/non-invert cursor is easily implemented by programming the CRTC for a blinking cursor and externally inverting the video signal with an exclusive-OR gate

PROGRAMMABLE REGISTERS

The four programmable registers allow the MPU to position the cursor anywhere on the screen and allow the start address to be modified

The Address Register is a five-bit write-only register used as an "indirect" or "pointer" register Its contents are the address of one of the other 18 registers When both RS and $\overline{CS}$ are low, the Address Register is selected When $\overline{CS}$ is low and RS is high, the register pointed to by the Address Register is selected

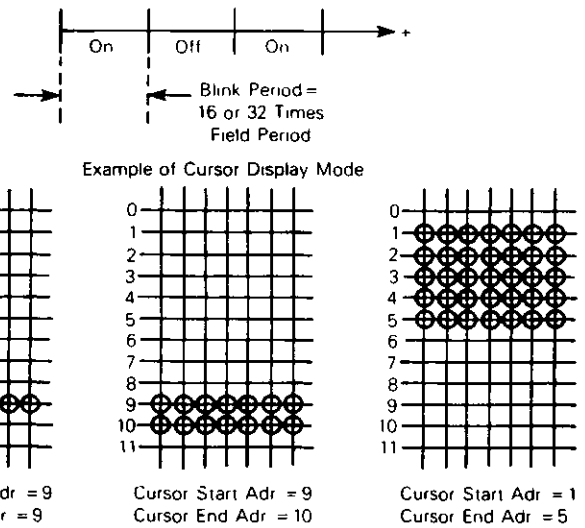
Start Address Register (R12-H, R13-L) — This 14-bit write-only register pair controls the first address output by the CRTC after vertical blanking It consists of an 8-bit low order (MA0-MA7) register and a 6-bit high order (MA8-MA13) register The start address register determines which portion of the refresh RAM is displayed on the CRT screen Hardware scrolling by character, line or page may be accomplished by modifying the contents of this register

Cursor Register (R14-H, R15-L) — This 14-bit write-only register pair is programmed to position the cursor anywhere in the refresh RAM area thus allowing hardware paging and scrolling through memory without loss of the original cursor position It consists of an 8-bit low order (MA0-MA7) register and a 6-bit high order (MA8-MA13) register

CRTC INITIALIZATION

Registers R12-R15 must be initialized after the system is powered up The processor will normally load the CRTC register file from a firmware table Figure 15 shows an M6800 program which could be used to program the CRT Controller

FIGURE 14 — CURSOR CONTROL



ADDITIONAL CRTC APPLICATIONS

The foremost system function which may be performed by the CRTC controller is the refreshing of dynamic RAM. This is quite simple as the refresh addresses continually run.

Both the VS and the HS outputs may be used as a real time clock. Once programmed, the CRTC will provide a stable reference frequency.

SELECTING MASK PROGRAMMED REGISTER VALUES

A prototype system may be developed using the MC6845 CRTC. This will allow register values to be modified as required to meet system specifications. The worksheet of Table 5 is extremely useful in computing proper register values for the MC6835. The program shown in Figure 15 may be expanded to properly load the calculated register values in the MC6845. Once the two sets of register values have been developed, fill out the ROM program worksheet of Figure 18.

To order a custom programmed MC6835, contact your local field service office, local sales person or your local Motorola representative. A manufacturing mask will be developed for the data entered in Figure 18.

FIGURE 15 — M6800 PROGRAM FOR CRTC INITIALIZATION

```
PAGE  001  CRTCINIT.SA:1  MC6835 CRTC initialization program

00001                          NAM     MC6835
00002                          TTL     CRTC initialization program
00003                          OPT     G,S,LLE=85 print FCB'x, FDB's & XREF table
00004                    ********************************************************
00005                    * Assign CRTC address
00006                    *
00007          9000  A CRTCAD EQU     $9000    Address Register
00008          9001  A CRTCRG EQU     CRTCAD+1 Data Register
00009                    ********************************************************
00010                    * Initialization Program
00011                    *
00012A 0000                    ORG     0        a place to start
00013A 0000 C6 0C    A         LDAB    $C       initialize pointer
00014A 0002 CE 1020  A         LDX     38RTTAB  table pointer
00015A 0005 F7 9000  A CRTC1   STAB    CRTCAD   load address register
00016A 0008 A6 00    A         LDAA    0,X      get register value from table
00017A 000A B7 9001  A         STAA    CRTCRG   program register
00018A 000D 08                 INX             increment counter
00019A 000E 5C                 INCB
00020A 000F D1 10    A         CMPB    $10      finished?
00021A 0011 26 F2 0005         BNE     CRTC1    no: take branch
00022A 0013 3F                 SWI             yes: call monitor
00023                    ********************************************************
00024                    * CRTC register initialization table
00025                    *
00026A 1020                    ORG     $1020    start of table
00027A 1020    0080  A CRTTAB  FDB     $0080    R12, R13 - Start Address
00028A 1022    0080  A         FDB     $0080    R14, R15 - Cursor Address
00029                          END
TOTAL ERRORS 00000--00000


CRTC1  0005  CRTCAD 9000  CRTCRG 9001  CRTTAB 1020
```

TABLE 5 — CRTC FORMAT WORKSHEET

Display Format Worksheet

1	Displayed Characters per Row		_____	Char
2	Displayed Character Rows per Screen		_____	Rows
3	Character Matrix	a Columns	_____	Columns
		b Rows	_____	Rows
4	Character Block	a Columns	_____	Columns
		b Rows	_____	Rows
5	Frame Refresh Rate		_____	Hz
6	Horizontal Oscillator Frequency		_____	Hz
7	Active Scan Lines (Line 2 × Line 4b)		_____	Lines
8	Total Scan Lines (Line 6 – Line 5)		_____	Lines
9	Total Rows Per Screen (Line 8 ÷ Line 4b)		_____ Rows	and _____ Lines
10	Vertical Sync Delay (Char Rows)		_____	Rows
11	Vertical Sync Width (Scan Lines (16))		_____	Lines
12	Horizontal Sync Delay (Character Times)		_____	Char Times
13	Horizontal Sync Width (Character Times)		_____	Char Times
14	Horizontal Scan Delay (Character Times)		_____	Char Times
15	Total Character Times (Line 1 + 12 + 13 + 14)		_____	Char Times
16	Character Rate (Line 6 × 15)		_____	Hz
17	Dot Clock Rate (Line 4a × 16)		_____	Hz

CRTC Registers

		Decimal	Hex
R0	Horizontal Total (Line 15 – 1)	_____	_____
R1	Horizontal Displayed (Line 1)	_____	_____
R2	Horizontal Sync Position (Line 1 + Line 12)	_____	_____
R3	Horizontal Sync Width (Line 13)	_____	_____
R4	Vertical Total (Line 9 – 1)	_____	_____
R5	Vertical Adjust (Line 9 Lines)	_____	_____
R6	Vertical Displayed (Line 2)	_____	_____
R7	Vertical Sync Position (Line 2 + Line 10)	_____	_____
R8	Interlace (00 Normal, 01 Interlace, 03 Interlace, and Video)		_____
R9	Max Scan Line Add (Line 4b – 1)	_____	_____
R10	Cursor Start	_____	_____
R11	Cursor End	_____	_____
R12, R13	Start Address (H and L)	_____	_____
R14, R15	Cursor (H and L)		_____

TABLE 6 — WORKSHEET FOR 80×24 FORMAT

Display Format Worksheet

1	Displayed Characters per Row		80	Char
2	Displayed Character Rows per Screen		24	Rows
3	Character Matrix	a Columns	7	Columns
		b Rows	9	Rows
4	Character Block	a Columns	9	Columns
		b Rows	11	Rows
5	Frame Refresh Rate		60	Hz
6	Horizontal Oscillator Frequency		18 600	Hz
7	Active Scan Lines (Line 2 × Line 4b)		264	Lines
8	Total Scan Lines (Line 6 – Line 5)		310	Lines
9	Total Rows Per Screen (Line 8 – Line 4b)		28 Rows and 2	Lines
10	Vertical Sync Delay (Char Rows)			Rows
11	Vertical Sync Width (Scan Lines (16))		16	Lines
12	Horizontal Sync Delay (Character Times)		6	Char Times
13	Horizontal Sync Width (Character Times)		9	Char Times
14	Horizontal Scan Delay (Character Times)		7	Char Times
15	Total Character Times (Line 1 + 12 + 13 + 14)		102	Char Times
16	Character Rate (Line 6 times 15)		1 8972 M	MHz
17	Dot Clock Rate (Line 4a times 16)		17 075 M	MHz

CRTC Registers

			Decimal	Hex
R0		Horizontal Total (Line 15 minus 1)	101	65
R1		Horizontal Displayed (Line 1)	80	50
R2		Horizontal Sync Position (Line 1 + Line 12)	86	56
R3		Horizontal Sync Width (Line 13)	9	9
R4		Vertical Total (Line 9 minus 1)	27	18
R5		Vertical Adjust (Line 9 Lines)	2	0A
R6		Vertical Displayed (Line 2)	24	18
R7		Vertical Sync Position (Line 2 + Line 10)	24	18
R8		Interlace (00 Normal 01 Interlace, 03 Interlace and Video)		0
R9		Max Scan Line Add (Line 4b minus 1)	10	B
R10		Cursor Start	0	0
R11		Cursor End	11	B
R12	R13	Start Address (H and L)	128	00
				80
R14	R15	Cursor (H and L)	128	00
				80

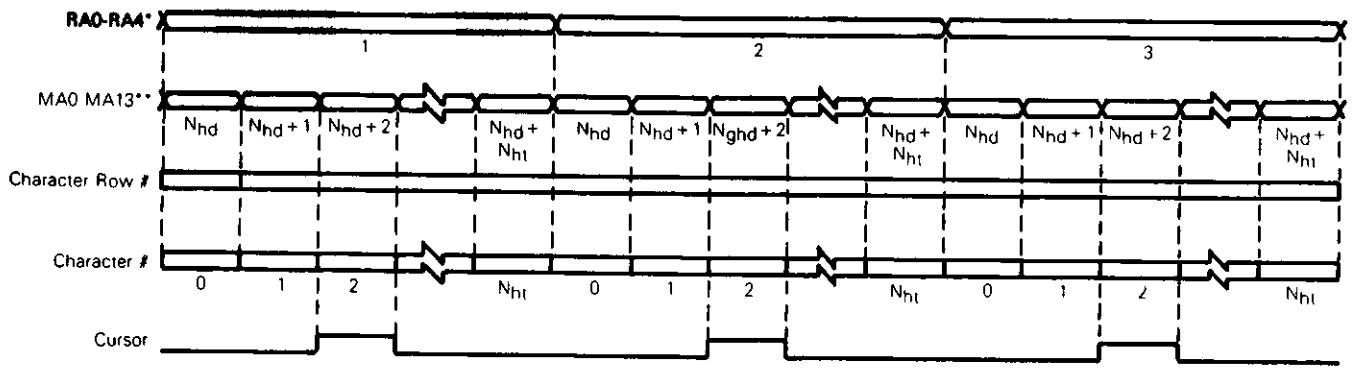
OPERATION OF THE CRTC

Timing of the CRT Interface Signals – Timing charts of CRT interface signals are illustrated in this section with the aid of programmed example of the CRTC. When values listed in Table 7 are programmed into CRTC control registers, the device provides the outputs as shown in the Timing Diagrams (Figures 11, 12, 16, and 17). The screen format of this example is shown in Figure 10. Figure 17 is an illustration of the relation between Refresh Memory Address (MA0-MA13), Raster Address (RA0-RA4) and the position on the screen. In this example, the start address is assumed to be "0".

TABLE 7 – VALUES PROGRAMMED INTO CRTC REGISTERS

Register Number	Register Name	Value	Programmed Value
R0	H Total	$N_{ht}+1$	N_{ht}
R1	H Displayed	N_{hd}	N_{hd}
R2	H Sync Position	N_{hsp}	N_{hsp}
R3	H Sync Width	N_{hsw}	N_{hsw}
R4	V Total	$N_{vt}+1$	N_{vt}
R5	V Scan Line Adjust	N_{adj}	N_{adj}
R6	V Displayed	N_{vd}	N_{vd}
R7	V Sync Position	N_{vsp}	N_{vsp}
R8	Interlace Mode		
R9	Max Scan Line Address	N_{sl}	N_{sl}
R10	Cursor Start		
R11	Cursor End		
R12	Start Address (H)	0	
R13	Start Address (L)	0	
R14	Cursor (H)		
R15	Cursor (L)		

FIGURE 16 – CURSOR TIMING

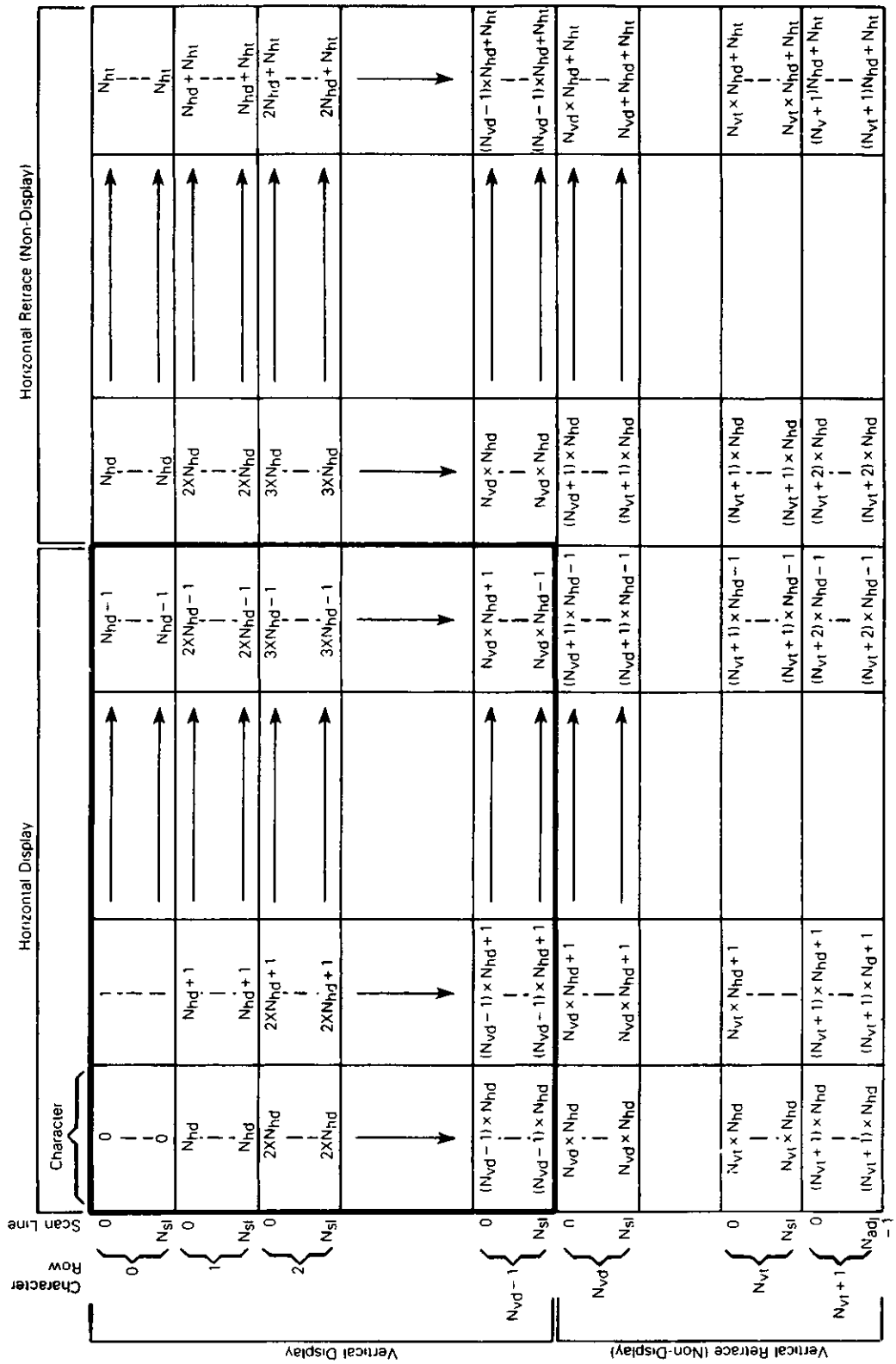


*Timing is shown for non interlace and interlace sync modes
Example shown has cursor programmed as
Cursor Register = N_{hd} + 2
Cursor Start = 1
Cursor End = 3

**The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0

NOTE 1 Timing values are described in Table 8

FIGURE 17 — REFRESH MEMORY ADDRESSING (MA0-MA13) STATE CHART



NOTE 1 The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/R13 = 0. Only Non-Interlace and Interlace Sync Modes are shown.

FIGURE 18 — ROM PROGRAM WORKSHEET

The value in each register of the MC6845 should be entered without any modifications. Motorola will take care of translating into the appropriate format.

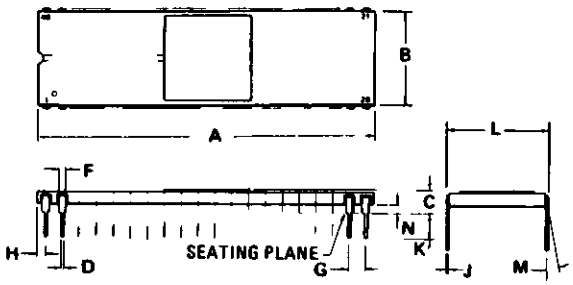
☐ All numbers are in decimal. ☐ All numbers are in hex.

	ROM Program Zero (PROG = 0)	ROM Program One (PROG = 1)
R0		
R1		
R2		
R3		
R4		
R5		
R6		
R7		
R8		
R9		
R10		
R11		

ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Ceramic L Suffix	1.0	0°C to 70°C	MC6835L
	1.0	−50°C to 85°C	MC6835CL
	1.5	0°C to 70°C	MC68A35L
	1.5	−50°C to 85°C	MC68A35CL
	2.0	0°C to 70°C	MC68B35L
	2.0	−50°C to 85°C	MC68B35CL
Cerdip S Suffix	1.0	0°C to 70°C	MC6835S
	1.0	−50°C to 85°C	MC6835CS
	1.5	0°C to 70°C	MC68A35S
	1.5	−50°C to 85°C	MC68A35CS
	2.0	0°C to 70°C	MC68B35S
	2.0	−50°C to 85°C	MC68B35CS
Plastic P Suffix	1.0	0°C to 70°C	MC6835P
	1.0	−50°C to 85°C	MC6835CP
	1.5	0°C to 70°C	MC68A35P
	1.5	−50°C to 85°C	MC68A35CP
	2.0	0°C to 70°C	MC68B35P
	2.0	−50°C to 85°C	MC68B35CP

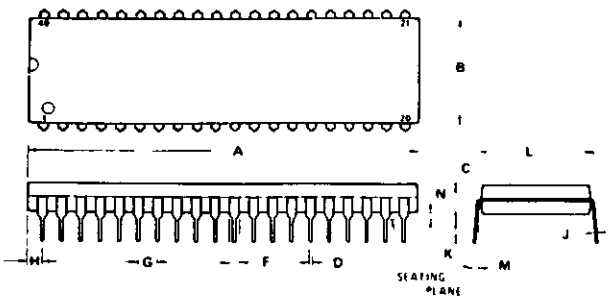
PACKAGE DIMENSIONS



L SUFFIX
CERAMIC PACKAGE
CASE 715-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50 29	51 31	1 980	2 020
B	14 94	15 34	0 588	0 604
C	3 05	4 06	0 120	0 160
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 99	15 49	0 590	0 610
M	–	10°	–	10°
N	1 02	1 52	0 040	0 060

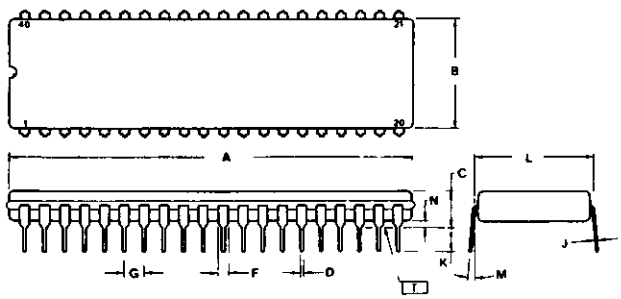
NOTES
1 LEADS TRUE POSITIONED WITHIN 0 25 mm (0 010) DIA (AT SEATING PLANE) AT MAX MAT L CONDITION
2 DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL



P SUFFIX
PLASTIC PACKAGE
CASE 711-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51 69	52 45	2 035	2 065
B	13 72	14 22	0 540	0 560
C	3 94	5 08	0 155	0 200
D	0 36	0 56	0 014	0 022
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 38	0 008	0 015
K	2 92	3 43	0 115	0 135
L	15 24 BSC		0 600 BSC	
M	0°	15°	0°	15°
N	0 51	1 02	0 020	0 040

NOTES
1 POSITIONAL TOLERANCE OF LEADS (D) SHALL BE WITHIN 0 25 mm (0 010) AT MAXIMUM MATERIAL CONDITION IN RELATION TO SEATING PLANE AND EACH OTHER
2 DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL
3 DIMENSION B DOES NOT INCLUDE MOLD FLASH



S SUFFIX
CERDIP PACKAGE
CASE 734-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51 31	53 24	2 020	2 096
B	12 70	15 49	0 500	0 610
C	4 06	5 84	0 160	0 230
D	0 38	0 56	0 015	0 022
F	1 27	1 65	0 050	0 065
G	2 54 BSC		0 100 BSC	
J	0 20	0 30	0 008	0 012
K	3 18	4 06	0 125	0 160
L	15 24 BSC		0 600 BSC	
M	5°	15°	5°	15°
N	0 51	1 27	0 020	0 050

NOTES
1 DIMENSION A IS DATUM
2 POSITIONAL TOLERANCE FOR LEADS
⌖ | ⌀0 25 (0 010) Ⓜ | T | A Ⓜ
3 T IS SEATING PLANE
4 DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL
5 DIMENSION A AND B INCLUDES MENISCUS

MOTOROLA *Semiconductor Products Inc.*
3501 ED BLUESTEIN BLVD AUSTIN TEXAS 78721 • A SUBSIDIARY OF MOTOROLA INC

BR1941(5016) Dual Baud Rate Clock

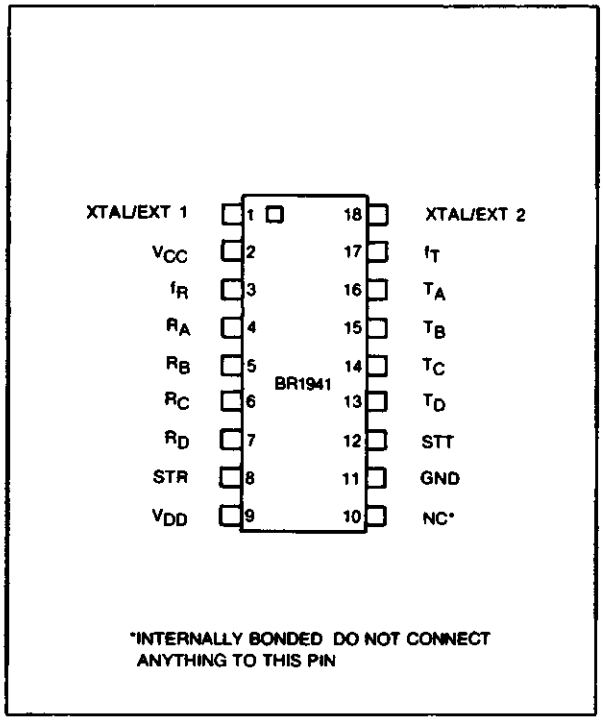
FEATURES

- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES
- SELECTABLE 1X, 16X OR 32X CLOCK OUTPUTS FOR FULL DUPLEX OPERATIONS
- OPERATES WITH CRYSTAL OSCILLATOR OR EXTERNALLY GENERATED FREQUENCY INPUT
- ROM MASKABLE FOR NON-STANDARD FREQUENCY SELECTIONS
- INTERFACES EASILY WITH MICROCOMPUTERS
- OUTPUTS A 50% DUTY CYCLE CLOCK WITH 0.01% ACCURACY
- 6 DIFFERENT FREQUENCY/DIVISOR PAIRS AVAILABLE
- TTL, MOS COMPATIBILITY
- PIN COMPATIBLE WITH COM5016

GENERAL DESCRIPTION

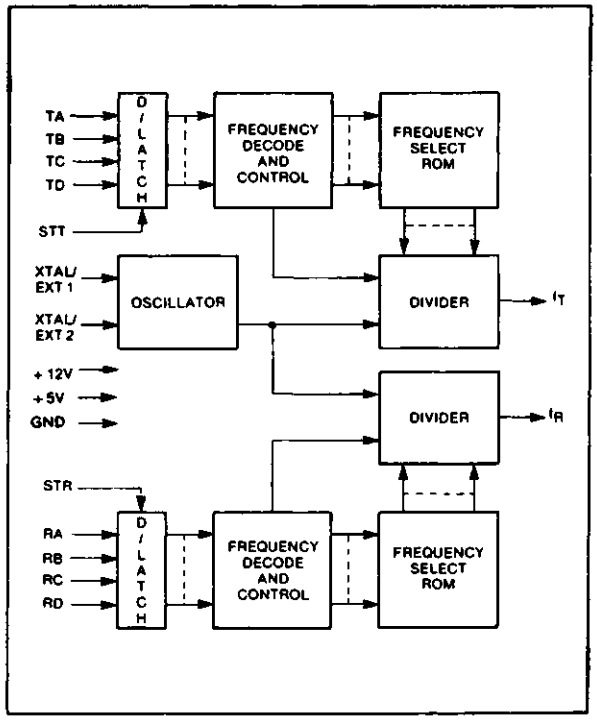
The BR1941 is a combination Baud Rate Clock Generator and Programmable Divider. It is manufactured in N-channel MOS using silicon gate technology. This device is capable of generating 16 externally selected clock rates whose frequency is determined by either a single crystal or an externally generated input clock. The BR1941 is a programmable counter capable of generating a division from 2 to $(2^{15} - 1)$.

The BR1941 is available programmed with the most used frequencies in data communication. Each frequency is selectable by strobing or hard wiring each of the two sets of four Rate Select inputs. Other frequencies/division rates can be generated by reprogramming the internal ROM coding through a MOS mask change. Additionally, further clock division may be accomplished through cascading of devices. The frequency output is fed into the XTAL/EXT input on a subsequent device.



*INTERNALLY BONDED DO NOT CONNECT ANYTHING TO THIS PIN

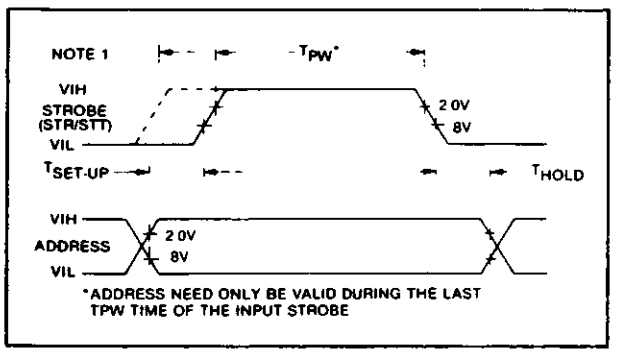
PIN CONNECTIONS



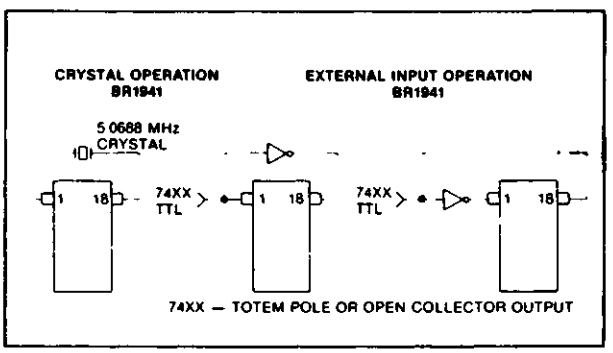
BR1941 BLOCK DIAGRAM

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	XTAL/EXT 1	Crystal or External Input 1	This input receives one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt. Supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver Address inputs.
4-7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs as shown in Tables 1 through 6, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register. This input may be strobed or hard wired to +5V.
9	V_{DD}	Power Supply	+12 volt Supply
10	NC	No Connection	Internally bonded. Do not connect anything to this pin.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wired to +5V.
13-16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Tables 1 through 6, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter Address inputs.
18	XTAL/EXT 2	Crystal or External Input 2	This input receives the other pin of the crystal package or the other polarity of the external input.



CONTROL TIMING



CRYSTAL/CLOCK OPTIONS

ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin, with respect to ground	+20.0V
Negative Voltage on any Pin, with respect to ground	−0.3V
Storage Temperature	(plastic package) −55°C to +125°C (cerdip package and ceramic package) −65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+325°C

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and Functional Operation of the device at these or at any other condition above those indicated in the operational sections of this specification are not implied.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	See Note 1
High-level, V_{IH}	V_{CC} – 1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 3.2 mA
High-level, V_{OH}	V_{CC} – 1.5	4.0		V	I_{OH} = 100µA
INPUT CURRENT					
Low-level, I_{IL}			0.3	mA	V_{IN} = GND, excluding XTAL inputs
INPUT CAPACITANCE					
All Inputs, C_{IN}		5	10	pf	V_{IN} = GND, excluding XTAL inputs
INPUT RESISTANCE					
Crystal Input, R_{XTAL}	1.1			KΩ	Resistance to ground for Pin 1 and Pin 18
POWER SUPPLY CURRENT					
I_{CC}		20	60	mA	
I_{DD}		20	70	mA	
AC CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY					See Note 2
PULSE WIDTH (T_{PW})					
Clock					50% duty cycle ± 10%. See Note 2
Receiver strobe	150		DC	ns	
Transmitter strobe	150		DC	ns	
INPUT SET-UP TIME (T_{SET-UP})					
Address	50			ns	See Note 3
OUTPUT HOLD TIME (T_{HOLD})					
Address	50			ns	

NOTE 1: BR1941 — XTAL/EXT inputs are either TTL compatible or crystal compatible. See crystal specification in Applications Information section.
All inputs except XTAL/EXT have internal pull-up resistors.

NOTE 2: Refer to frequency option tables for maximum input frequency on XTAL/EXT pins.
Typical Clock Pulse width is 1/2xCL.

NOTE 3: Input set-up time can be decreased to ≥0 ns by increasing the minimum strobe width by 50 ns to a total of 200 ns.

OPERATION

Standard Frequencies

Choose a Transmitter and Receiver frequency from the table below. Program the corresponding address into TA-TD and RA-RD respectively using strobe pulses or by hard wiring the strobe and address inputs.

Non-Standard Frequencies

To accomplish non-standard frequencies do one of the following:

1. Choose a crystal that when divided by the BR1941 generates the desired frequency.
2. Cascade devices by using the frequency outputs as an

input to the XTAL/EXT inputs of the subsequent BR1941.

3. Consult the factory for possible changes via ROM mask reprogramming.

FREQUENCY OPTIONS

TABLE 1. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

BR1941-00

TABLE 2. CLOCK FREQUENCY = 2.76480 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	3456
0	0	0	1	75	1.2	1.2	—	50/50	2304
0	0	1	0	110	1.76	1.76	- 0.006	50/50	1571
0	0	1	1	134.5	2.152	2.152	- 0.019	50/50	1285
0	1	0	0	150	2.4	2.4	—	50/50	1152
0	1	0	1	200	3.2	3.2	—	50/50	864
0	1	1	0	300	4.8	4.8	—	50/50	576
0	1	1	1	600	9.6	9.6	—	50/50	288
1	0	0	0	1200	19.2	19.2	—	50/50	144
1	0	0	1	1800	28.8	28.8	—	50/50	96
1	0	1	0	2000	32.0	32.15	+ 0.465	50/50	86
1	0	1	1	2400	38.4	38.4	—	50/50	72
1	1	0	0	3600	57.6	57.6	—	50/50	48
1	1	0	1	4800	76.8	76.8	—	50/50	36
1	1	1	0	9600	153.6	153.6	—	50/50	18
1	1	1	1	19,200	307.2	307.2	—	50/50	9

BR1941-02

TABLE 3. CRYSTAL FREQUENCY = 6.018305 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	.7999	0	50/50	7523*
0	0	0	1	75	1.2	1.2000	0	50/50	5015*
0	0	1	0	110	1.76	1.7597	0	50/50	3420
0	0	1	1	134.5	2.152	2.1517	0	50/50	2797*
0	1	0	0	150	2.4	2.3996	0	50/50	2508
0	1	0	1	200	3.2	3.1995	0	50/50	1881*
0	1	1	0	300	4.8	4.7993	0	50/50	1254
0	1	1	1	600	9.6	9.5986	0	50/50	627*
1	0	0	0	1200	19.2	19.2279	+ 0.14	50/50	31.3*
1	0	0	1	1800	28.8	28.7959	0	50/50	209*
1	0	1	0	2000	32.0	32.0125	0	50/50	188
1	0	1	1	2400	38.4	38.3334	- 0.17	50/50	157*
1	1	0	0	3600	57.6	57.8687	+ 0.46	50/50	104
1	1	0	1	4800	76.8	77.1583	+ 0.46	50/50	78
1	1	1	0	9800	153.6	154.3166	+ 0.46	50/50	39*
1	1	1	1	19,200	307.2	300.9175	- 2.04	50/50	20

BR1941-03

TABLE 4. CLOCK FREQUENCY = 5.52960 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	1.6	1.6	—	50/50	3456
0	0	0	1	75	2.4	2.4	—	50/50	2304
0	0	1	0	110	3.52	3.52	- 0.006	50/50	1571
0	0	1	1	134.5	4.304	4.303	- 0.019	50/50	1285
0	1	0	0	150	4.8	4.8	—	50/50	1152
0	1	0	1	200	6.4	6.4	—	50/50	864
0	1	1	0	300	9.6	9.6	—	50/50	576
0	1	1	1	600	19.2	19.2	—	50/50	288
1	0	0	0	1200	38.4	38.4	—	50/50	144
1	0	0	1	1800	57.6	57.6	—	50/50	96
1	0	1	0	2000	64.0	64.3	+ 0.465	50/50	86
1	0	1	1	2400	76.8	76.8	—	50/50	72
1	1	0	0	3600	115.2	115.2	—	50/50	48
1	1	0	1	4800	153.6	153.6	—	50/50	36
1	1	1	0	9600	307.2	307.2	—	50/50	18
1	1	1	1	19,200	614.4	614.4	—	50/50	9

BR1941-04

TABLE 5. CRYSTAL FREQUENCY = 4.9152 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(32X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7598	- 0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	- 0.19	*	171
1	0	0	1	2000	32.0	31.9168	- 0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	- 0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

BR1941-05

TABLE 6. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(32X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	1.6	1.6	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.303	.026	50/50	1178
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	298.16	2.941	*	17
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

*When the duty cycle is not exactly 50% it is 50% ± 10%

BR1941-06

CRYSTAL SPECIFICATIONS

User must specify termination (pin, wire, other)
Frequency — See Tables 1-6.
Temperature range 0°C to +70°C
Series resistance ≤ 50Ω
Series resonant
Overall tolerance ± .01%

CRYSTAL MANUFACTURERS (Partial List)

American Time Products Div.
Frequency Control Products, Inc.
61-20 Woodside Ave.
Woodside, New York 11377
(212) 458-5811

Bliley Electric Co.
2545 Grandview Blvd.
Erie, Pennsylvania 16508
(814) 838-3571

M-tron Ind. Inc.
P.O. Box 630
Yankton, South Dakota 57078
(605) 665-9321

Erie Frequency Control
453 Lincoln St.
Calisle, Pennsylvania 17013
(714) 249-2232

APPLICATIONS INFORMATION

OPERATION WITH A CRYSTAL

The BR1941 Baud Rate Generator may be driven by either a crystal or TTL level clock. When using a crystal, the waveform that appears at pins 1 (XTAL/EXT 1) and 18 (XTAL/EXT 2) does not conform to the normal TTL limits of $V_{IL} \leq 0.8V$ and $V_{IH} \geq 2.0V$. Figure 1 illustrates a typical crystal waveform when connected to a BR1941.

Since the D.C. level of the waveform causes the least positive point to typically be greater than 0.8V, the BR1941 is designed to look for an edge, as opposed to a TTL level. The XTAL/EXT logic triggers on a rising edge of typically 1V in magnitude. This allows the use of a crystal without any additional components.

OPERATIONS WITH TTL LEVEL CLOCK

With clock frequencies in the area of 5 MHz, significant overshoot and undershoot ("ringing") can appear at pins 1 and/or 18. The BR1941, may, at times, be triggered on a rising edge of an overshoot or undershoot waveform, causing the device to effectively "double-trigger." This phenomenon may result as a twice expected baud rate, or as an apparent device failure. Figure 2 shows a typical waveform that exhibits the "ringing" problem.

The design methods required to minimize ringing include the following:

1. Minimize the P.C. trace length. At 5 MHz, each inch of trace can add significantly to overshoot and undershoot.
2. Match impedances at both ends of the trace. For example, a series resistor near the BR1941 may be helpful.
3. A uniform impedance is important. This can be accomplished through the use of:
   a. parallel ground lines
   b. evenly spaced ground lines crossing the trace on the opposite side of PC board
   c. an inner plane of ground, e.g., as in a four layered PC board.

In the event that ringing exists on an already finished board, several techniques can be used to reduce it. These are:

1. Add a series resistor to match impedance as shown in Figure 3.
2. Add pull-up/pull-down resistor to match impedance, as shown in Figure 4.
3. Add a high speed diode to clamp undershoot, as shown in Figure 5.

The method that is easiest to implement in many systems is method 1, the series resistor. The series resistor will cause the D.C. level to shift up, but that does not cause a problem since the BR1941 is triggered by an edge, as opposed to a TTL level.

The BR1941 Baud Rate Generator can save both board space and cost in a communications system. By choosing either a crystal or a TTL level clock, the user can minimize the logic required to provide baud rate clocks in a given design.

POWER LINE SPIKES

Voltage transients on the AC power line may appear on the DC power output. If this possibility exists, it is suggested that one by-pass capacitor is used between +5V and GND and another between +12V and GND.

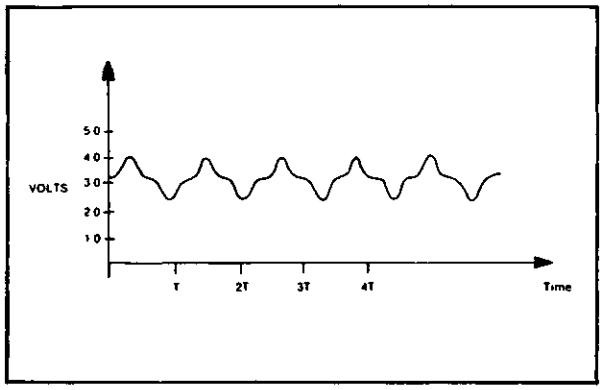


Figure 1 TYPICAL CRYSTAL WAVEFORM

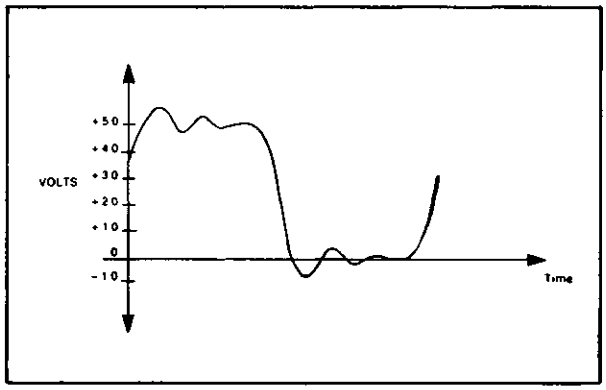


Figure 2 TYPICAL "RINGING" WAVEFORM

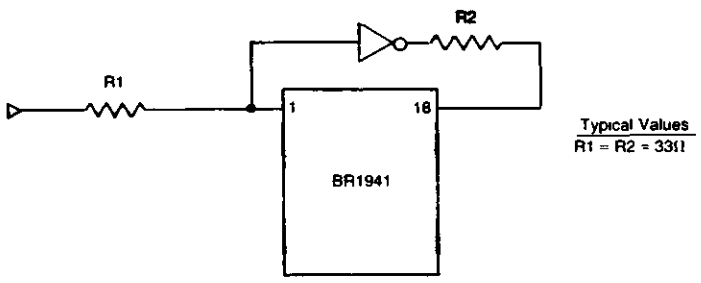


Figure 3 SERIES RESISTOR TO MATCH IMPEDANCE

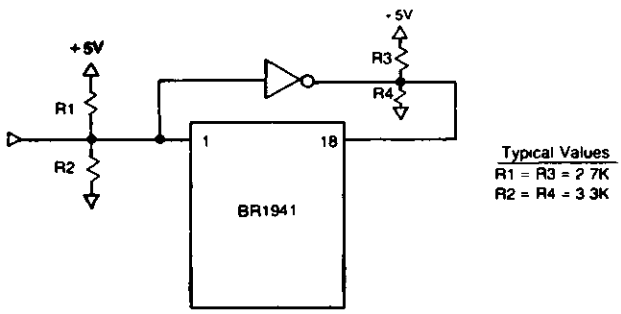


Figure 4 PULL-UP/PULL-DOWN RESISTORS TO MATCH IMPEDANCE

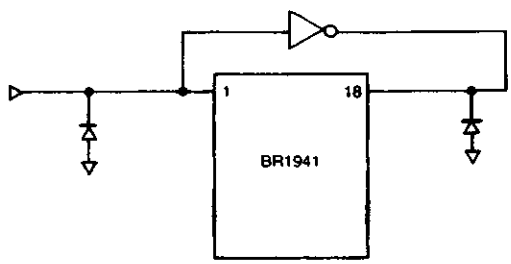


Figure 5 HIGH-SPEED DIODE TO CLAMP UNDERSHOOT

See page 725 for ordering information.

Printed in U S A

WD1943(8116)/WD1945(8136) Dual Baud Rate Clock

FEATURES

- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES
- OPERATES WITH CRYSTAL OSCILLATOR OR EXTERNALLY GENERATED FREQUENCY INPUT
- ROM MASKABLE FOR NON-STANDARD FREQUENCY SELECTIONS
- INTERFACES EASILY WITH MICROCOMPUTERS
- OUTPUTS A 50% DUTY CYCLE CLOCK WITH 0 01% ACCURACY
- 6 DIFFERENT FREQUENCY/DIVISOR PAIRS AVAILABLE
- SINGLE +5V POWER SUPPLY
- COMPATIBLE WITH BR1941
- TTL, MOS COMPATIBILITY

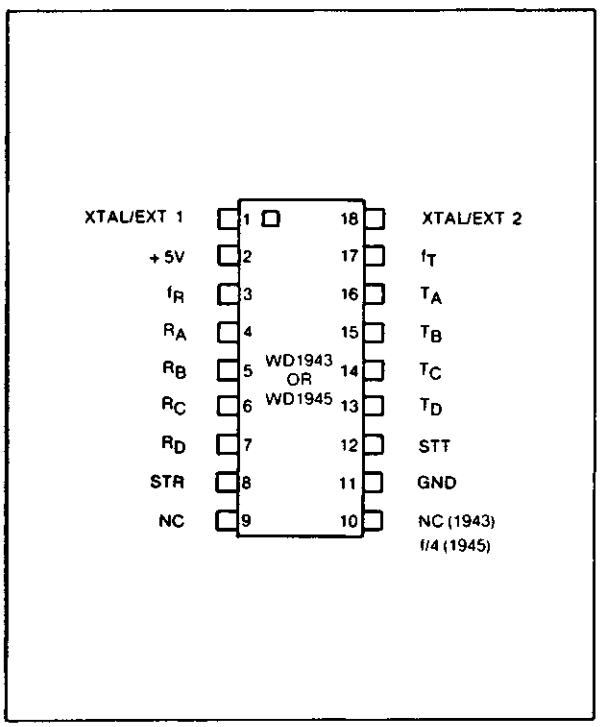
- WD1943 IS PIN COMPATIBLE TO THE COM8116
- WD1945 IS PIN COMPATIBLE TO THE COM8136 AND COM5036 (PIN 9 ON WD1945 IS A NO CONNECT)

GENERAL DESCRIPTION

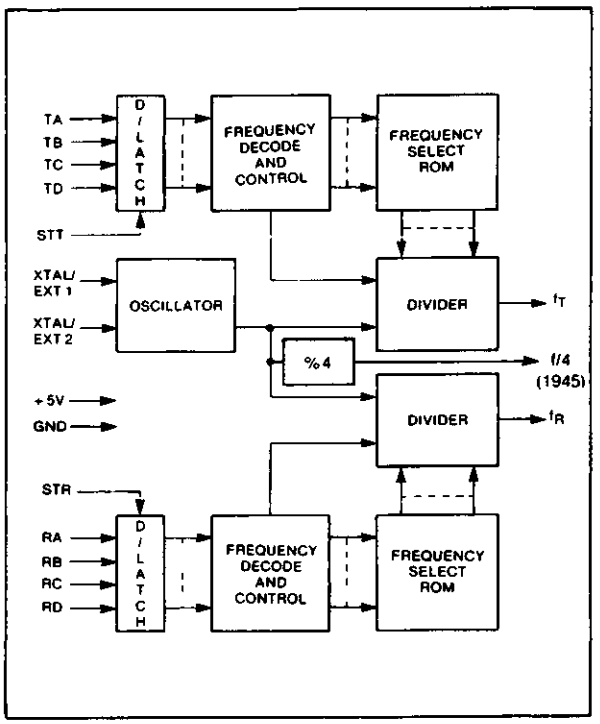
The WD1943/45 is an enhanced version of the BR1941 Dual Baud Rate Clock The WD1943/45 is a combination Baud Rate Clock Generator and Programmable Divider It is manufactured in N-channel MOS using silicon gate technology This device is capable of generating 16 externally selected clock rates whose frequency is determined by either a single crystal or an externally generated input clock The WD1943/45 is a programmable counter capable of generating a division by any integer from 4 to $2^{15} - 1$, inclusive

The WD1943/45 is available programmed with the most used frequencies in data communication Each frequency is selectable by strobing or hard wiring each of the two sets of four Rate Select inputs Other frequencies/division rates can be generated by reprogramming the internal ROM coding through a MOS mask change Additionally, further clock division may be accomplished through cascading of devices The frequency output is fed into the XTAL/EXT input on a subsequent device

The WD1943/45 can be driven by an external crystal or by TTL logic



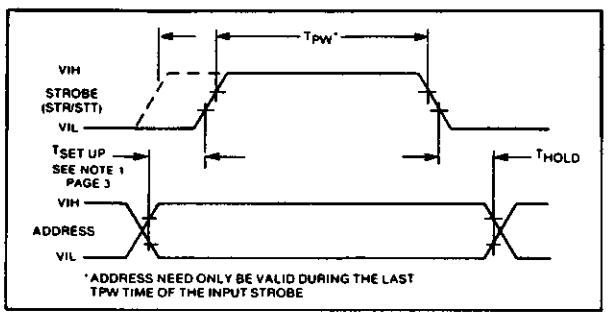
PIN CONNECTIONS



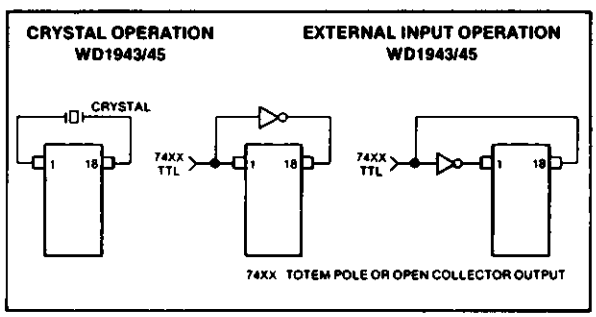
BLOCK DIAGRAM

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	XTAL/EXT 1	Crystal or External Input 1	This input receives one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+ 5 volt Supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver Address inputs.
4-7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs as shown in Table 1 thru 6, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register. This input may be strobed or hard wired to + 5V.
9	NC	No Connection	No Internal Connection
10	NC (1943) f/4 (1945)	No Connection freq/4 Output	No Internal Connection XTAL1 input freq divided by four.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wired to + 5V.
13-16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Table 1 thru 6, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter Address inputs.
18	XTAL/EXT 2	Crystal or External Input 2	This input receives the other pin of the crystal package or the other polarity of the external input.



CONTROL TIMING



CRYSTAL/CLOCK OPTIONS

ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin, with respect to ground	+ 7.0V
Negative Voltage on any Pin, with respect to ground	− 0.3V
Storage Temperature	(plastic package) − 55°C to + 125°C (Cerdip package and Ceramic package) − 65°C to + 150°C
Lead Temperature (Soldering, 10 sec.)	+ 325°C

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and Functional Operation of the device at these or at any other condition above those indicated in the operational sections of this specification are not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = +5V ±5% standard.)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	See Note 1
High-level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 3.2 mA
High-level, V_{OH}	V_{CC}-1.5	4.0		V	I_{OH} = 100μA
INPUT CURRENT			−10	μA	V_{IN} = V_{CC} STR (8) and STT (12)
High-level, I_{IH}			10	μA	V_{IN} = GND Only
Low-level, I_{IL}			300	μA	V_{IN} = GND (All inputs except XTAL, STR and STT)
Low-level, I_{IL}			10	μa	V_{IN} = GND STR, STT
INPUT CAPACITANCE					
All Inputs, C_{IN}		5	10	pf	V_{IN} = GND, excluding XTAL inputs
EXT. INPUT LOAD		4	5		Series 7400 unit loads
INPUT RESISTANCE					
Crystal Input, R_{XTAL}	1.1			KΩ	Resistance to ground for Pin 1 and Pin 18
POWER SUPPLY CURRENT I_{CC}		40	80	mA	
AC CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY					See Note 2
PULSE WIDTH (T_{PW})					
Clock					50% Duty Cycle ± 10%. See Note 2
Receiver strobe	150		DC	ns	See Note 3
Transmitter strobe	150		DC	ns	See Note 3
INPUT SET-UP TIME (T_{SET-UP})					
Address	50			ns	See Note 3
OUTPUT HOLD TIME (T_{HOLD})					
Address	50			ns	
STROBE TO NEW FREQUENCY DELAY			6	CLK	

NOTE 1: XTAL/EXT inputs are either TTL compatible or crystal compatible. See crystal specification in Applications Information section.
All inputs except XTAL, STR and STT have internal pull-up resistors.

NOTE 2: Refer to frequency option tables for maximum input frequency on XTAL/EXT pins.
Typical clock pulse width is 1/2 x CL

NOTE 3: Input set-up time can be decreased to >0 ns by increasing the minimum strobe width (50 ns) to a total of 200 ns.
T_{A-D} and R_{A-D} have internal pull-up resistors.

OPERATION

Standard Frequencies

Choose a Transmitter and Receiver frequency from the table below. Program the corresponding address into TA-TD and RA-RD respectively using strobe pulses or by hard wiring the strobe and address inputs.

Non-Standard Frequencies

To accomplish non-standard frequencies do one of the following:

1. Choose a crystal that when divided by the WD1943 generates the desired frequency.
2. Cascade devices by using the frequency outputs as an input to the XTAL/EXT inputs of the subsequent WD1943/45.
3. Consult the factory for possible changes via ROM mask reprogramming.

FREQUENCY OPTIONS

TABLE 1. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

WD1943-00 or WD1945-00

TABLE 2. CLOCK FREQUENCY = 2.76480 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	3456
0	0	0	1	75	1.2	1.2	—	50/50	2304
0	0	1	0	110	1.76	1.76	−0.006	50/50	1571
0	0	1	1	134.5	2.152	2.152	−0.019	50/50	1285
0	1	0	0	150	2.4	2.4	—	50/50	1152
0	1	0	1	200	3.2	3.2	—	50/50	864
0	1	1	0	300	4.8	4.8	—	50/50	576
0	1	1	1	600	9.6	9.6	—	50/50	288
1	0	0	0	1200	19.2	19.2	—	50/50	144
1	0	0	1	1800	28.8	28.8	—	50/50	96
1	0	1	0	2000	32.0	32.15	+0.465	50/50	86
1	0	1	1	2400	38.4	38.4	—	50/50	72
1	1	0	0	3600	57.6	57.6	—	50/50	48
1	1	0	1	4800	76.8	76.8	—	50/50	36
1	1	1	0	9600	153.6	153.6	—	50/50	18
1	1	1	1	19,200	307.2	307.2	—	50/50	9

WD1943-02 or WD1945-02

TABLE 3. CRYSTAL FREQUENCY = 6.018305 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	.7999	0	50/50	7523*
0	0	0	1	75	1.2	1.2000	0	50/50	5015*
0	0	1	0	110	1.76	1.7597	0	50/50	3420
0	0	1	1	134.5	2.152	2.1517	0	50/50	2797*
0	1	0	0	150	2.4	2.3996	0	50/50	2508
0	1	0	1	200	3.2	3.1995	0	50/50	1881*
0	1	1	0	300	4.8	4.7993	0	50/50	1254
0	1	1	1	600	9.6	9.5986	0	50/50	627*
1	0	0	0	1200	19.2	19.2279	+0.14	50/50	31.3*
1	0	0	1	1800	28.8	28.7959	0	50/50	209*
1	0	1	0	2000	32.0	32.0125	0	50/50	188
1	0	1	1	2400	38.4	38.3334	−0.17	50/50	157*
1	1	0	0	3600	57.6	57.8687	+0.46	50/50	104
1	1	0	1	4800	76.8	77.1583	+0.46	50/50	78
1	1	1	0	9800	153.6	154.3166	+0.46	50/50	39*
1	1	1	1	19,200	307.2	300.9175	−2.04	50/50	20

WD1943-03 or WD1945-03

TABLE 4. CLOCK FREQUENCY = 5.52960 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(32X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	1.6	1.6	—	50/50	3456
0	0	0	1	75	2.4	2.4	—	50/50	2304
0	0	1	0	110	3.52	3.52	−0.006	50/50	1571
0	0	1	1	134.5	4.304	4.303	−0.019	50/50	1285
0	1	0	0	150	4.8	4.8	—	50/50	1152
0	1	0	1	200	6.4	6.4	—	50/50	864
0	1	1	0	300	9.6	9.6	—	50/50	576
0	1	1	1	600	19.2	19.2	—	50/50	288
1	0	0	0	1200	38.4	38.4	—	50/50	144
1	0	0	1	1800	57.6	57.6	—	50/50	96
1	0	1	0	2000	64.0	64.3	+0.465	50/50	86
1	0	1	1	2400	76.8	76.8	—	50/50	72
1	1	0	0	3600	115.2	115.2	—	50/50	48
1	1	0	1	4800	153.6	153.6	—	50/50	36
1	1	1	0	9600	307.2	307.2	—	50/50	18
1	1	1	1	19,200	614.4	614.4	—	50/50	9

WD1943-04 or WD1945-04

TABLE 5. CRYSTAL FREQUENCY = 4.9152 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7598	−0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	−0.19	*	171
1	0	0	1	2000	32.0	31.9168	−0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	−0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

WD1943-05 or WD1945-05

TABLE 6. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(32X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	1.6	1.6	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.303	.026	50/50	1178
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	298.16	2.941	*	17
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

*When the duty cycle is not exactly 50% it is 50% ± 10%

WD1943-06 or WD1945-06

APPLICATIONS INFORMATION

OPERATION WITH A CRYSTAL

The WD1943/45 Baud Rate Generator may be driven by either a crystal or TTL level clock. When using a crystal, the waveform that appears at pins 1 (XTAL/EXT 1) and 18 (XTAL/EXT 2) does not conform to the normal TTL limits of $V_{IL} \leq 0.8V$ and $V_{IH} \geq 2.0V$. Figure 1 illustrates a typical crystal waveform when connected to a WD1943/45.

Since the D.C. level of the waveform causes the least positive point to typically be greater than 0.8V, the WD1943/45 is designed to look for an edge, as opposed to a TTL level. The XTAL/EXT logic triggers on a rising edge of typically 1V in magnitude. This allows the use of a crystal without any additional components.

OPERATIONS WITH TTL LEVEL CLOCK

With clock frequencies in the area of 5 MHz, significant overshoot and undershoot ("ringing") can appear at pins 1 and/or 18. The clock oscilator may, at times be triggered on a rising edge of an overshoot or undershoot waveform, causing the device to effectively "double-trigger." This phenomenon may result as a twice expected baud rate, or as an apparent device failure. Figure 2 shows a typical waveform that exhibits the "ringing" problem.

The design methods required to minimize ringing include the following:

1. Minimize the P.C. trace length. At 5 MHz, each inch of trace can add significantly to overshoot and undershoot.
2. Match impedances at both ends of the trace. For example, a series resistor near the device may be helpful.
3. A uniform impedance is important. This can be accomplished through the use of:
   a. parallel ground lines
   b. evenly spaced ground lines crossing the trace on the opposite side of PC board
   c. an inner plane of ground, e.g., as in a four layered PC board.

In the event that ringing exists on an already finished board, several techniques can be used to reduce it. These are:

1. Add a series resistor to match impedance as shown in Figure 3.
2. Add pull-up/pull-down resistor to match impedance, as shown in Figure 4.
3. Add a high speed diode to clamp undershoot, as shown in Figure 5.

The method that is easiest to implement in many systems is method 1, the series resistor. The series resistor will cause the D.C. level to shift up, but that does not cause a problem since the OSC is triggered by an edge, as opposed to a TTL level.

The 1943/45 Baud Rate Generator can save both board space and cost in a communications system. By choosing either a crystal or a TTL level clock, the user can minimize the logic required to provide baud rate clocks in a given design.

POWER LINE SPIKES

Voltage transients on the AC power line may appear on the DC power output. If this possibility exists, it is suggested that a by-pass capacitor is used between + 5V and GND.

CRYSTAL SPECIFICATIONS

User must specify termination (pin, wire, other)
Frequency — See Tables 1-6.
Temperature range 0°C to + 70°C
Series resistance ≤ 50Ω
Series resonant
Overall tolerance ± 0.01%

CRYSTAL MANUFACTURERS (Partial List)

American Time Products Div.
Frequency Control Products, Inc.
61-20 Woodside Ave.
Woodside, New York 11377
(213) 458-5811

Bliley Electric Co.
2545 Grandview Blvd.
Erie, Pennsylvania 16508
(814) 838-3571

M-tron Ind. Inc.
P.O. Box 630
Yankton, South Dakota 57078
(605) 665-9321

Erie Frequency Control
453 Lincoln St.
Calisle, Pennsylvania 17013
(714) 249-2232

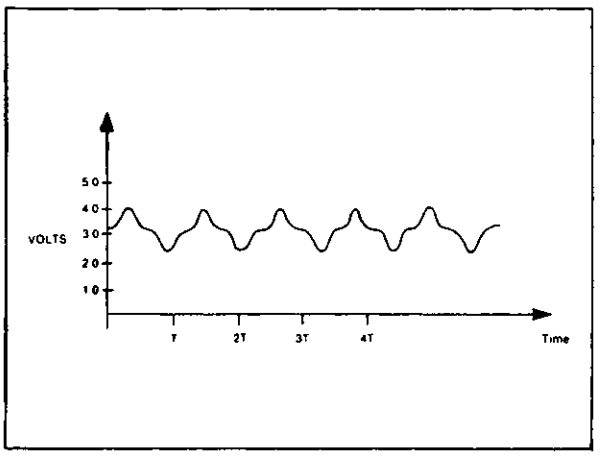


Figure 1. TYPICAL CRYSTAL WAVEFORM

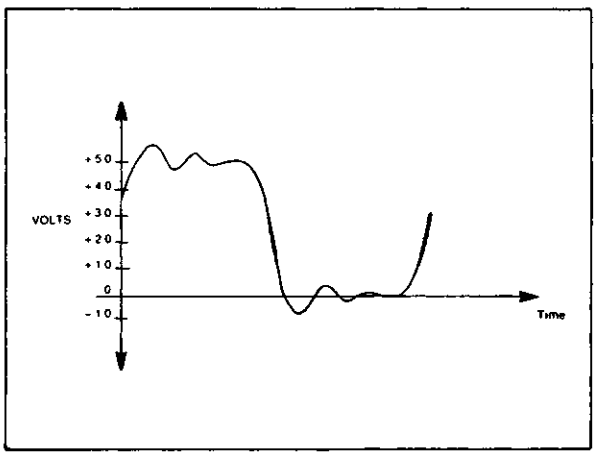


Figure 2. TYPICAL "RINGING" WAVEFORM from TTL INPUT

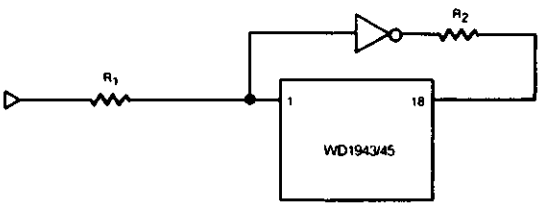


Figure 3. SERIES RESISTOR TO MATCH IMPEDANCE

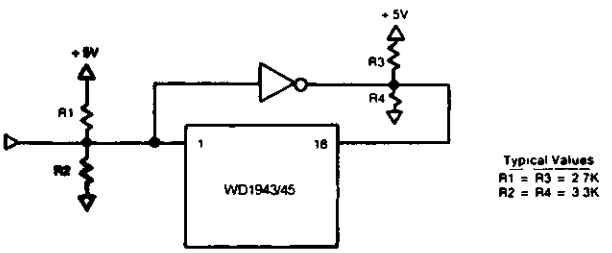


Figure 4. PULL-UP/PULL-DOWN RESISTORS TO MATCH IMPEDANCE

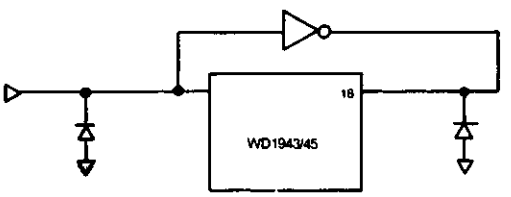


Figure 5. HIGH-SPEED DIODE TO CLAMP UNDERSHOOT

See page 725 for ordering information.

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WESTERN DIGITAL
CORPORATION

FD179X-02
Floppy Disk Formatter/Controller Family

FEATURES

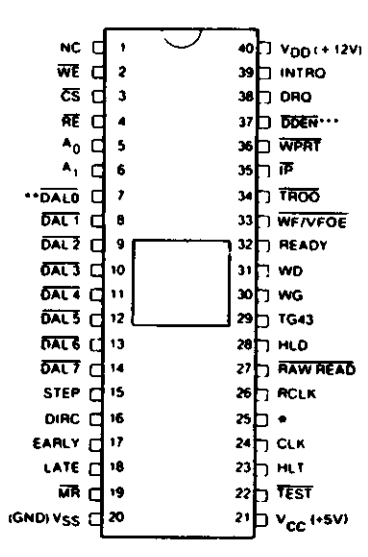
- TWO VFO CONTROL SIGNALS — RG & VFOE
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
  - Non IBM Format for Increased Capacity
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128, 256, 512 or 1024 Byte Sector Lengths
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- INTERFACES TO WD1691 DATA SEPARATOR
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1792	1793	1794	1795	1797
Single Density (FM)	X	X	X	X	X	X
Double Density (MFM)	X		X		X	X
True Data Bus			X	X		X
Inverted Data Bus	X	X			X	
Write Precomp	X	X	X	X	X	X
Side Selection Output					X	X

APPLICATIONS

8" FLOPPY AND 5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER



*1791/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS
***1792/4 OPEN

PIN DESIGNATION

FD179X SYSTEM BLOCK DIAGRAM

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$. Each line will drive 1 standard TTL load.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ± 1% for 8" drives, 1 MHz ±1% for mini-floppies.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occuring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.

$\overline{CS}$	A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	0	Status Reg	Command Reg
0	0	1	Track Reg	Track Reg
0	1	0	Sector Reg	Sector Reg
0	1	1	Data Reg	Data Reg

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated steppers.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.
25	READ GATE (1791, 1792, 1793, 1794)	RG	This output is used for synchronization of external data separators. The output goes high after two Bytes of zeros in single density, or 4 Bytes of either zeros or ones in double density operation.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 200 ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF/VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100K Ohm pull-up resistor.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
35	INDEX PULSE	$\overline{IP}$	This input informs the FD179X when the index hole is encountered on the diskette.
36	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	$\overline{DDEN}$	This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected. This line must be left open on the 1792/4.

GENERAL DESCRIPTION

The FD179X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is TTL compatible on all inputs and outputs. The outputs will drive ONE TTL load or three LS loads. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793 respectively. On these devices, DDEN must be left open.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input ($\overline{RAW\ READ}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

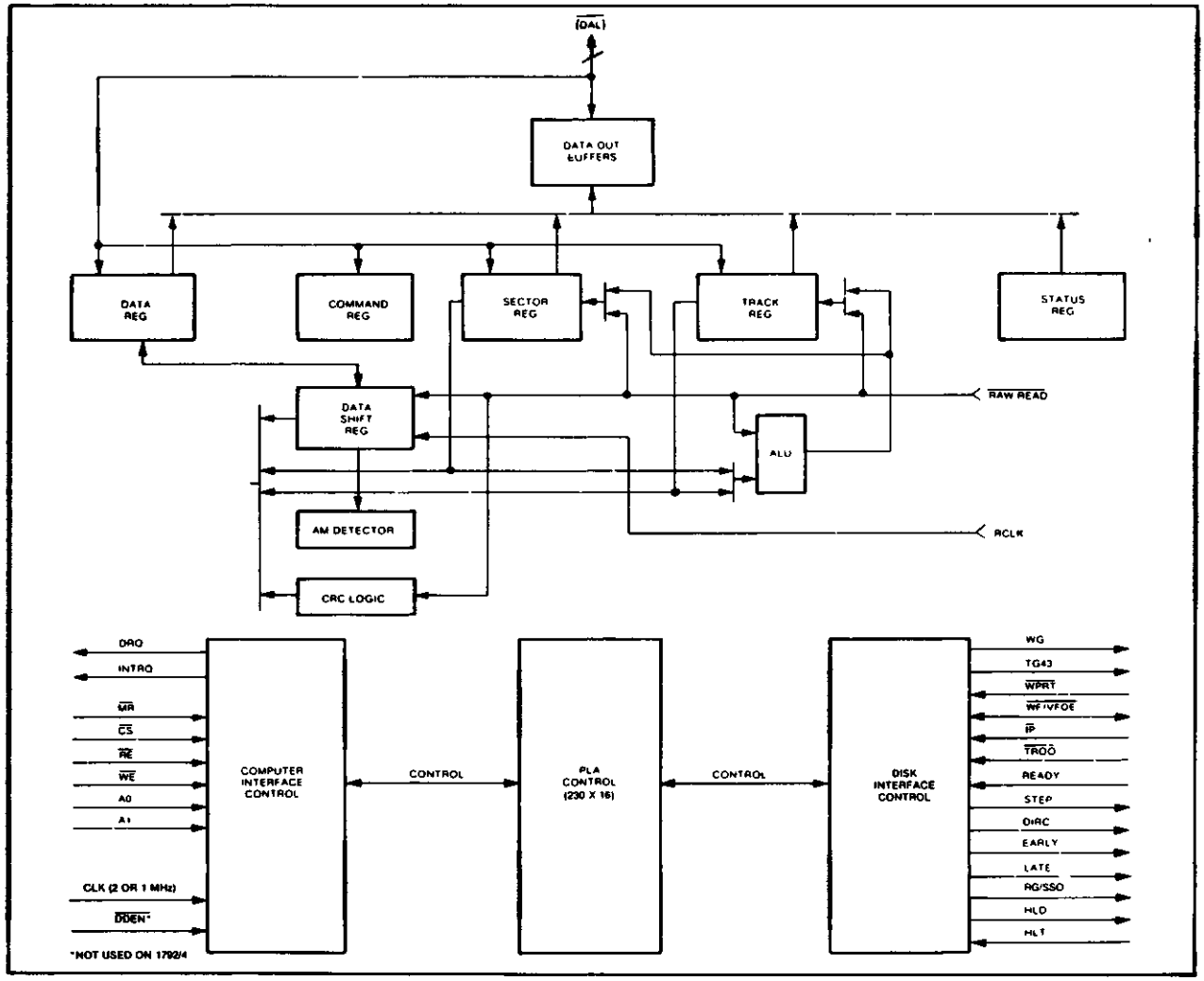
CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD179X has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single



FD179X BLOCK DIAGRAM

density (FM) is assumed. 1792 & 1794 are single density only.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data

Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*1795/97 may vary — see command summary.

The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table)

For read operations in 8" double density the FD179X requires $\overline{RAW\ READ}$ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1791/92/93/94 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{VFOE}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{VFOE}$ will go active low when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{WF}/\overline{VFOE}$ is not used, leave open or tie to a 10K resistor to +5.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{Write\ Fault}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{DDEN}$ = 1) and 200 ns pulses in MFM ($\overline{DDEN}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

READY

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 1791, 1792, 1793, 1794

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

B. Commands for Models: 1795, 1797

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TABLE 2. FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 1, Load head at beginning h = 0, Unload head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No 15 MS delay E = 1, 15 MS delay
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field: 00 / 01 / 10 / 11 L = 0: 256 / 512 / 1024 / 128 L = 1: 128 / 256 / 512 / 1024
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r0 r1), which determines the stepping motor rate as defined in Table 3.

A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK		2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$		0	1	0	1	x	x
R1	R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0	0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0	1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1	0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1	1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

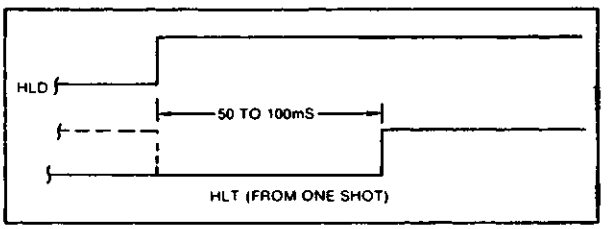
After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by settling bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

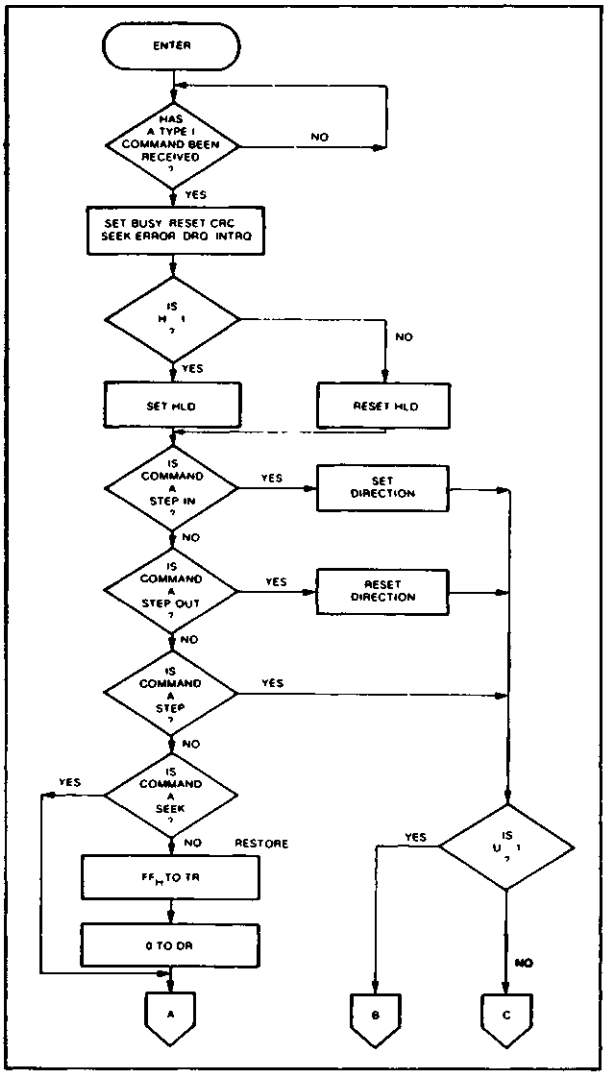
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

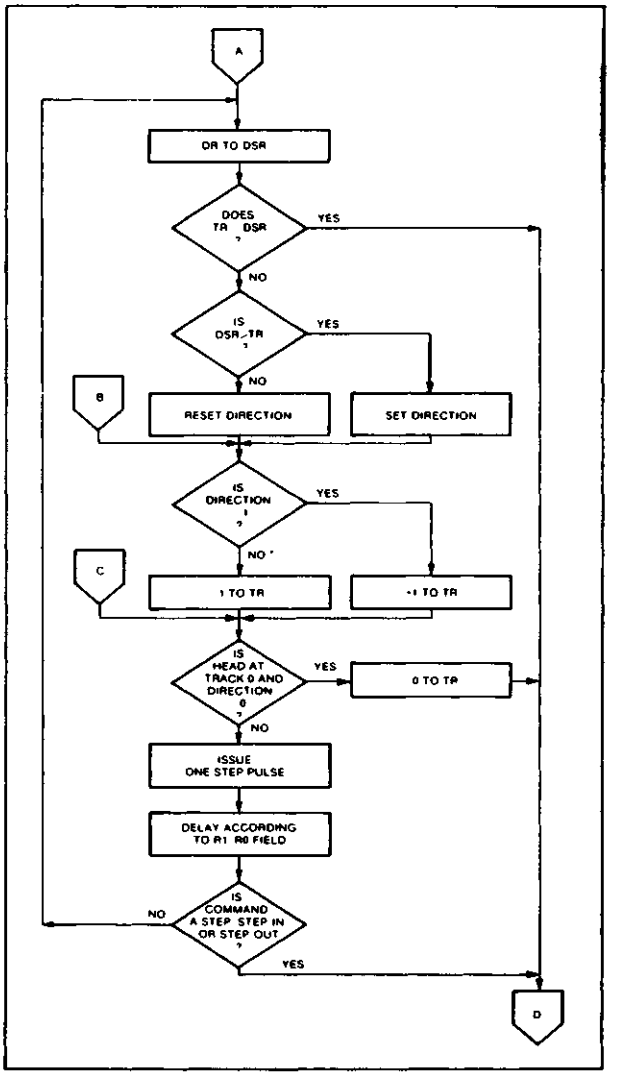
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r1 r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state and that the DRQ pin stays low.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

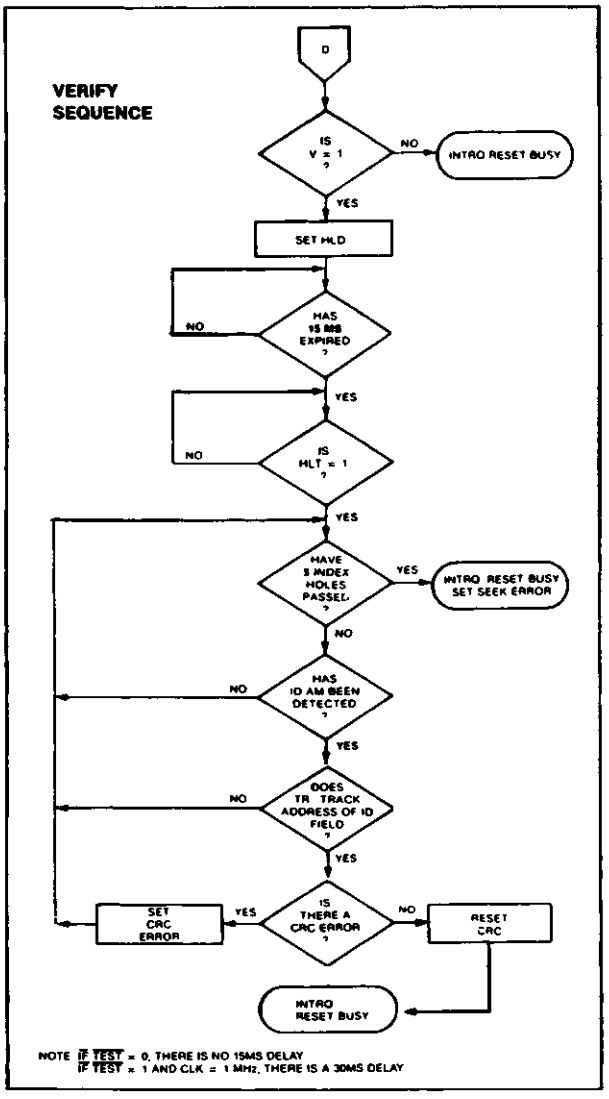
Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

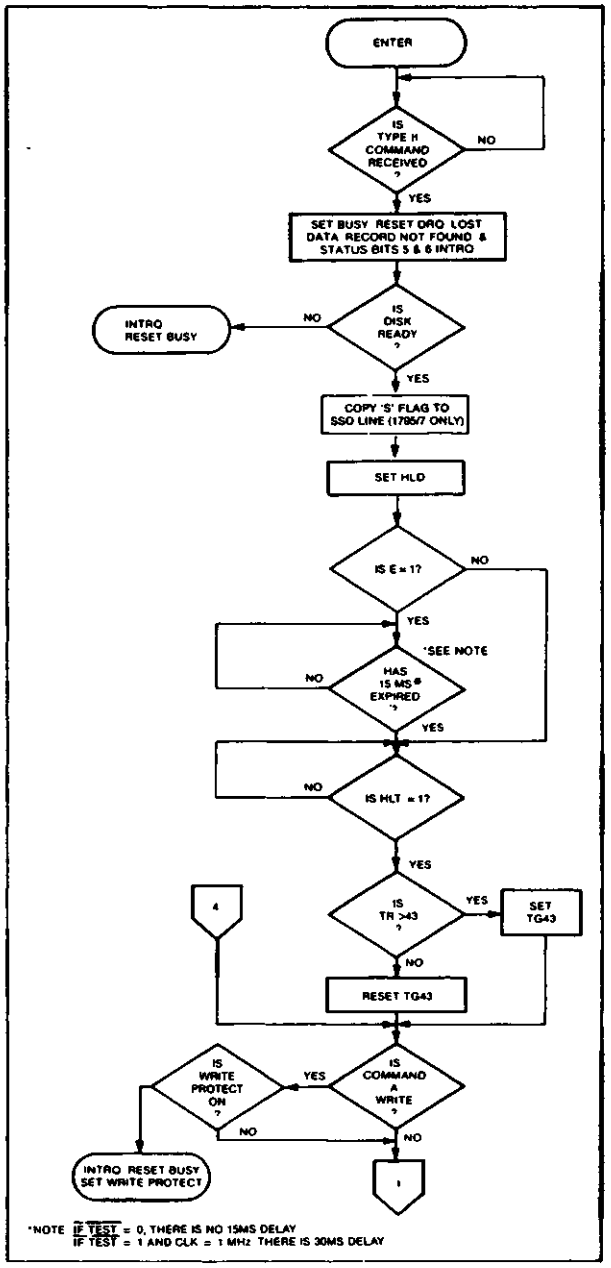


TYPE I COMMAND FLOW

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.



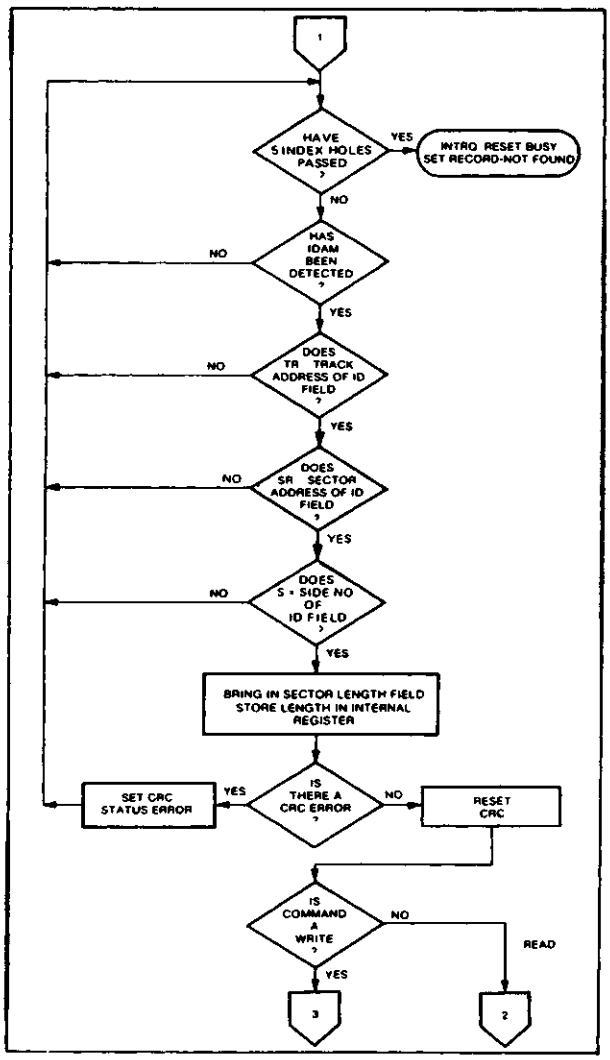
TYPE II COMMAND

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next

record. The FD179X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the FD179X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The FD179X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for 1791-94 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the FD179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.



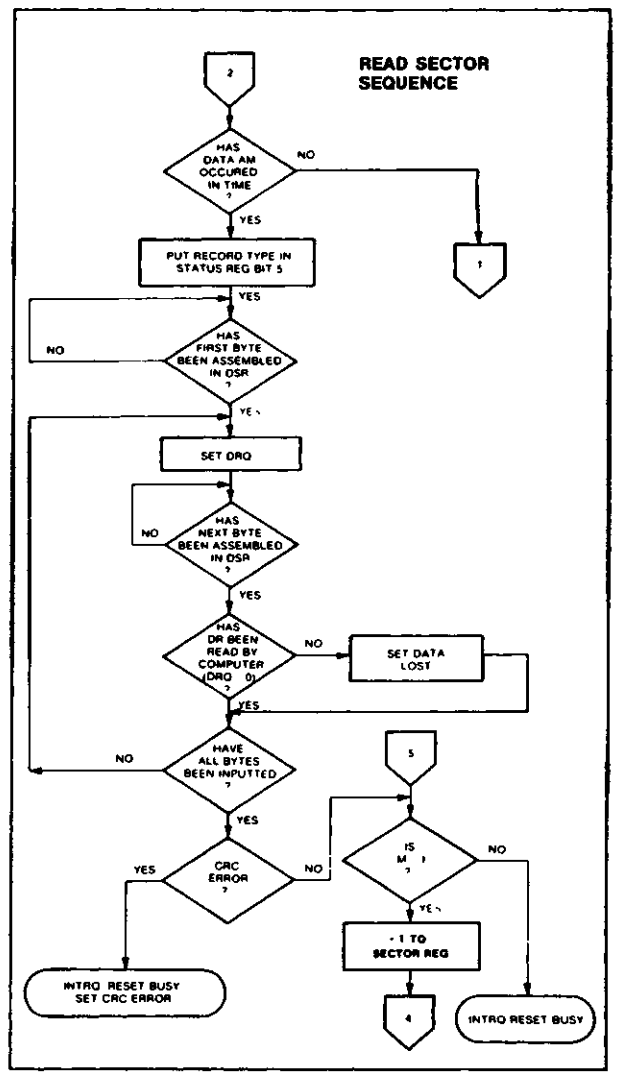
TYPE II COMMAND

The Type II and III commands for the 1795-97 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

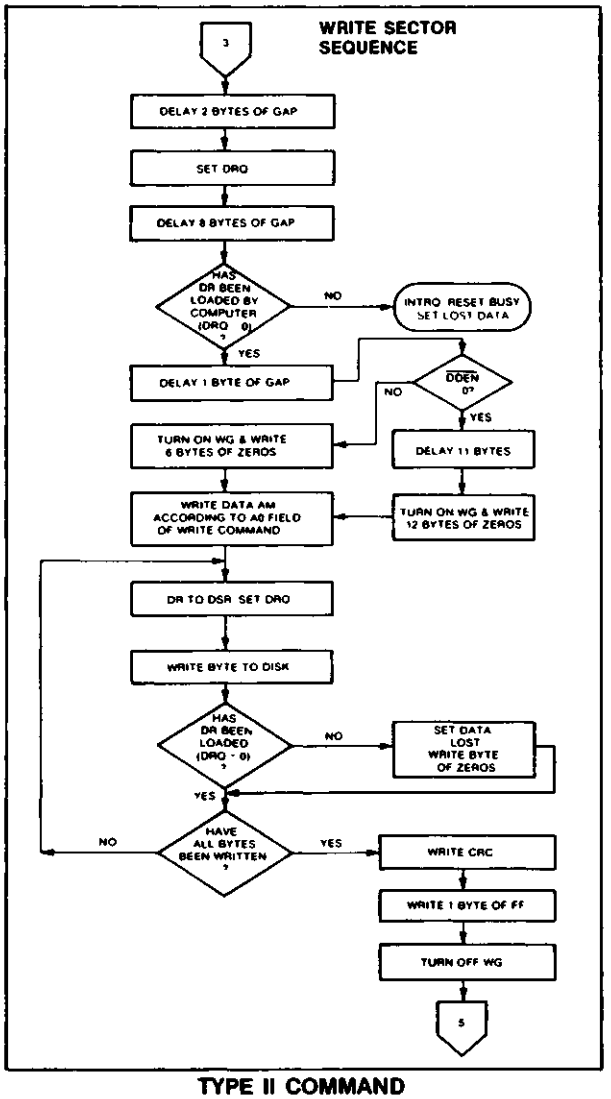
The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector.' For IBM compatability, the 'L' flag should be set to a one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address



TYPE II COMMAND



TYPE II COMMAND

Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field is searched for and verified again followed by the Data Address Mark search. If after 5 revolutions the DAM cannot be found, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

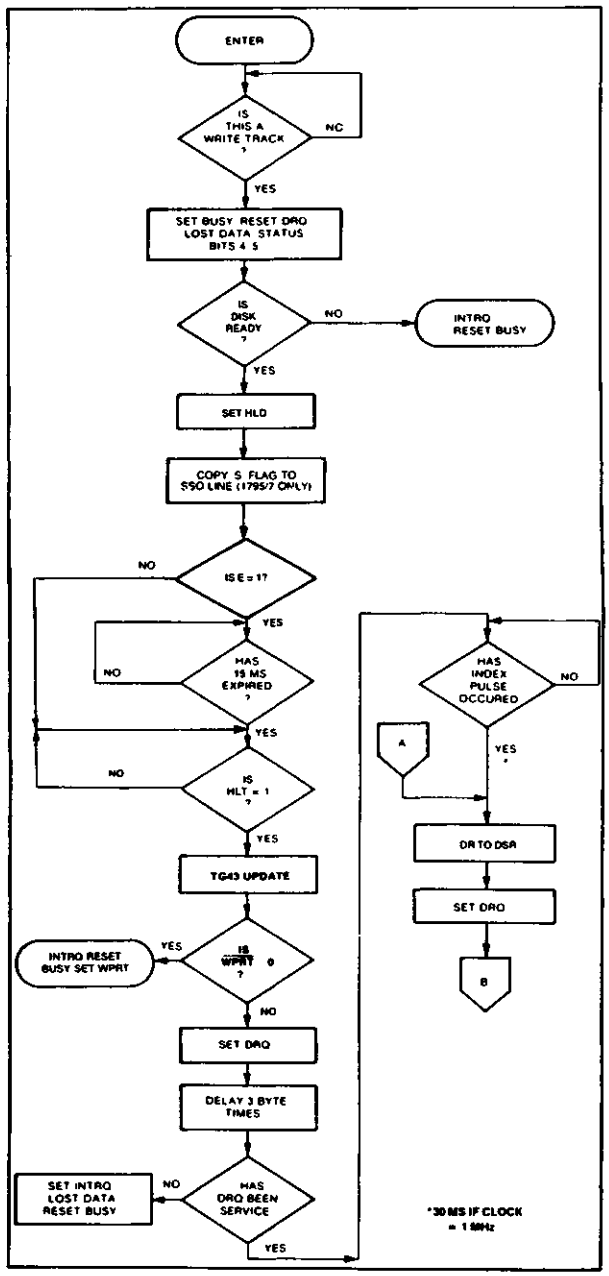
Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

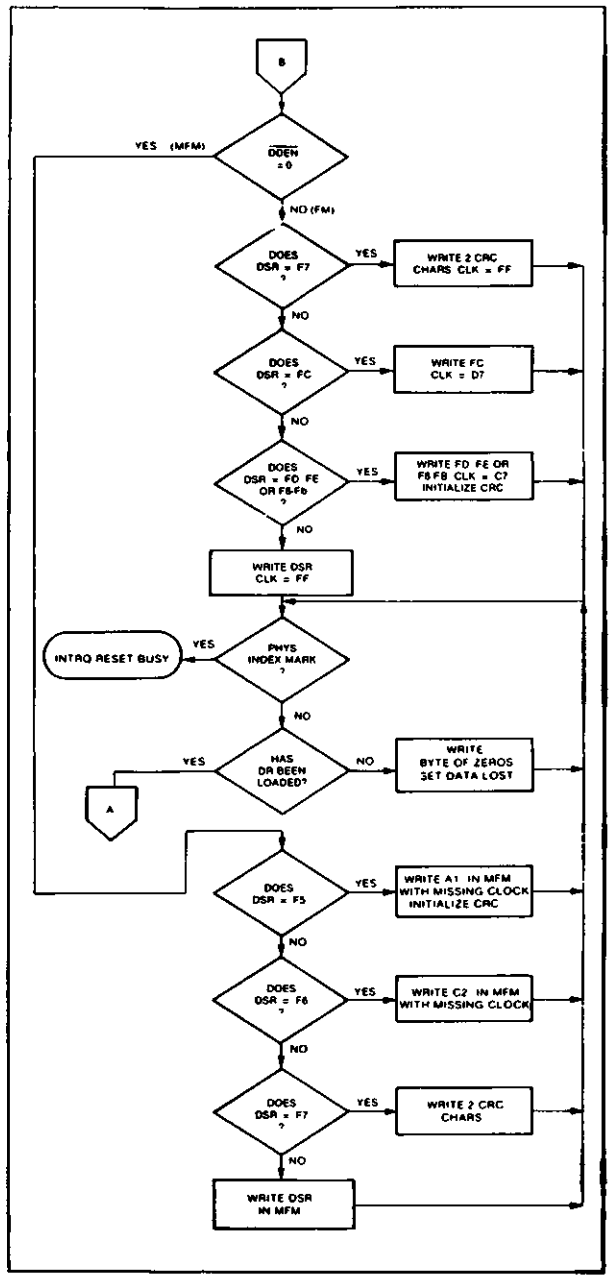
Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791/3 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 & 4

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

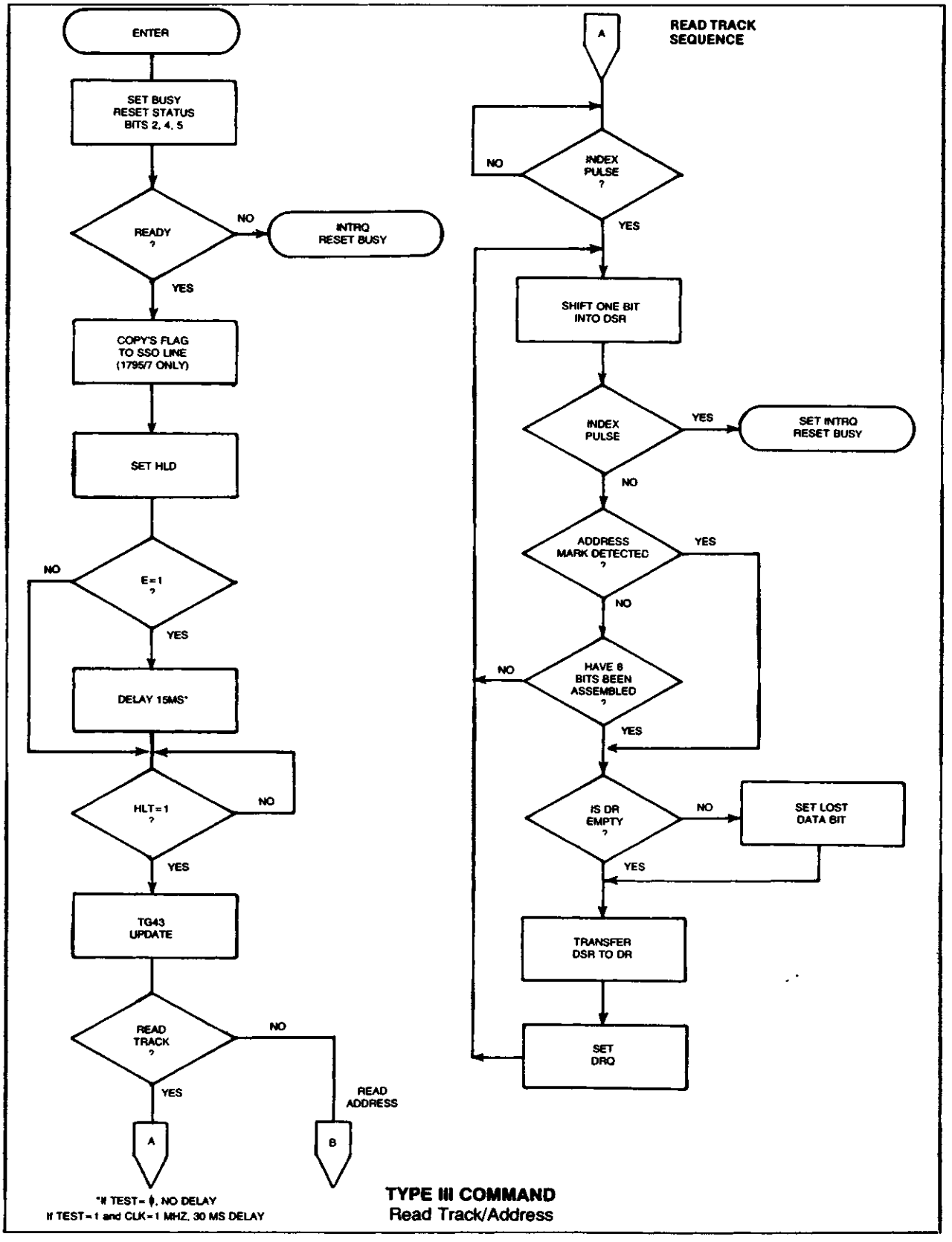
I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

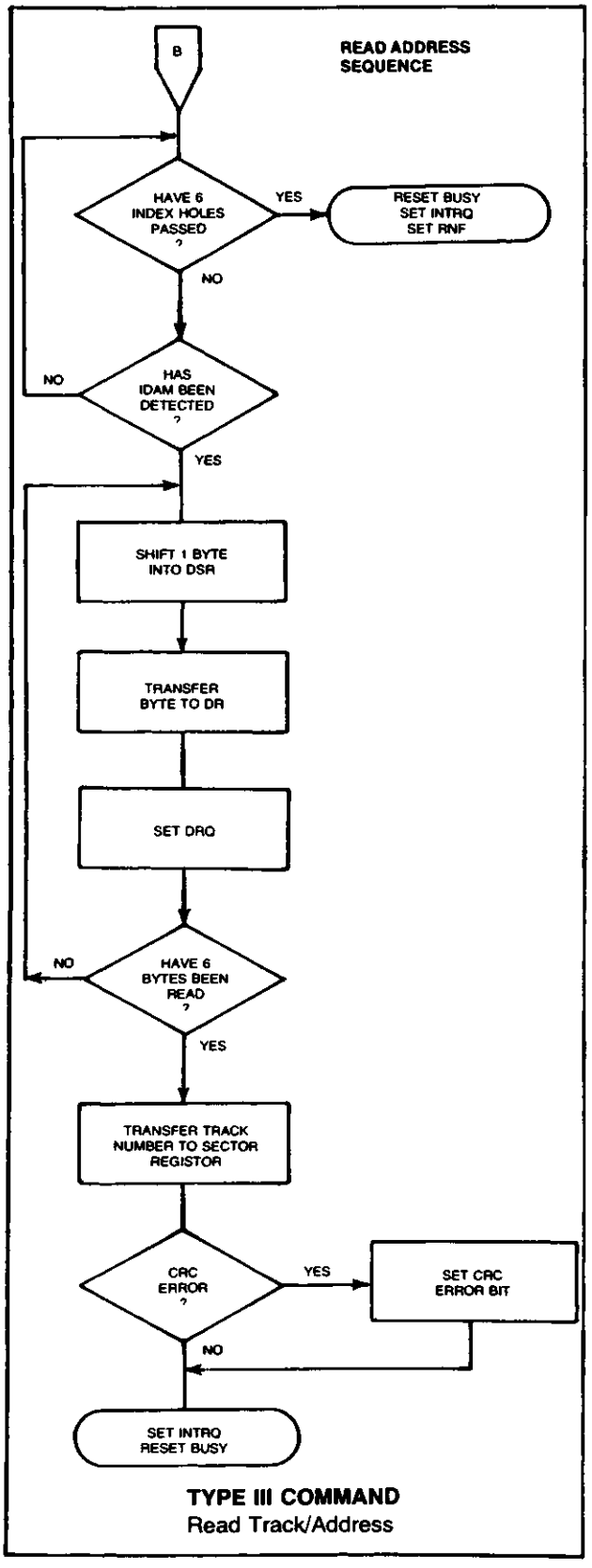
Wait 8 micro sec (double density) or 16 micro sec (single density before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT- READY or the next Index Pulse will cause an interrupt condition.



TYPE III COMMAND
Read Track/Address



TYPE III COMMAND
Read Track/Address

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 μs	6 μs
Write to Command Reg.	Read Status Bits 1-7	28 μs	14 μs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)[1]
6	00
1	FC (Index Mark)
* 26	FF (or 00)[1]
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)[1]
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)[1]
247**	FF (or 00)[1]

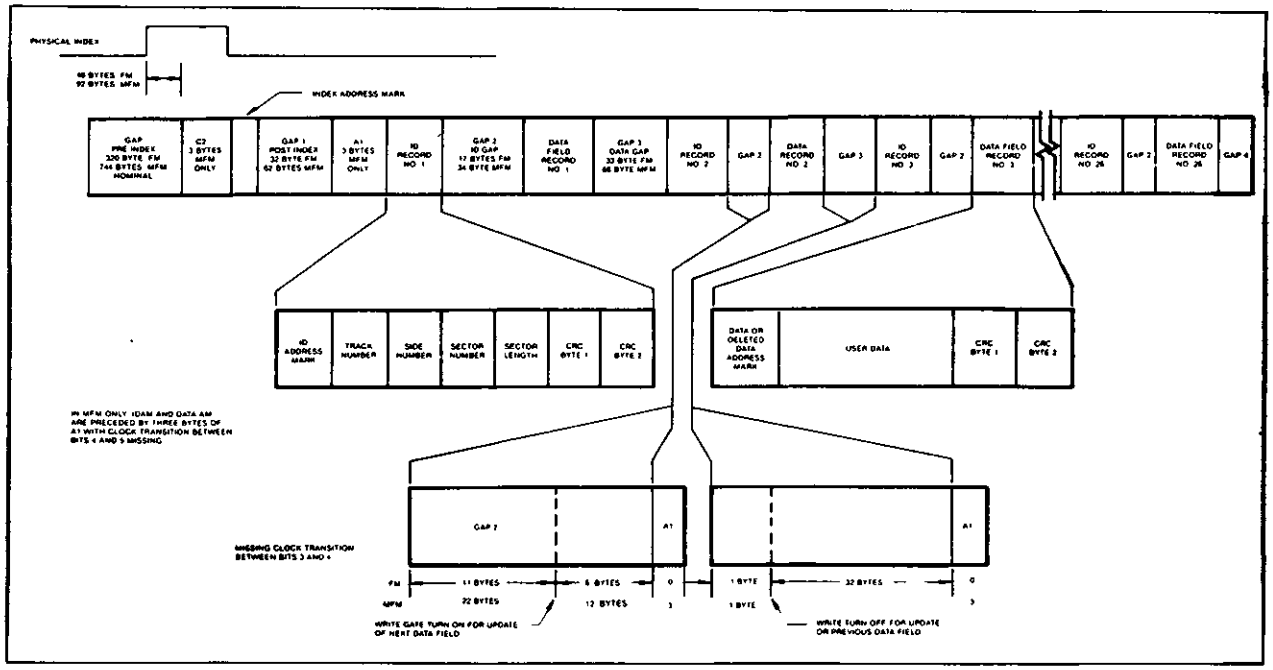
*Write bracketed field 26 times
**Continue writing until FD179X interrupts out.
Approx. 247 bytes.
1-Optional '00' on 1795/7 only.

IBM SYSTEM 34 FORMAT- 256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
* 50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

*Write bracketed field 26 times
**Continue writing until FD179X interrupts out.
Approx. 598 bytes.



IBM TRACK FORMAT

1. NON-IBM FORMATS

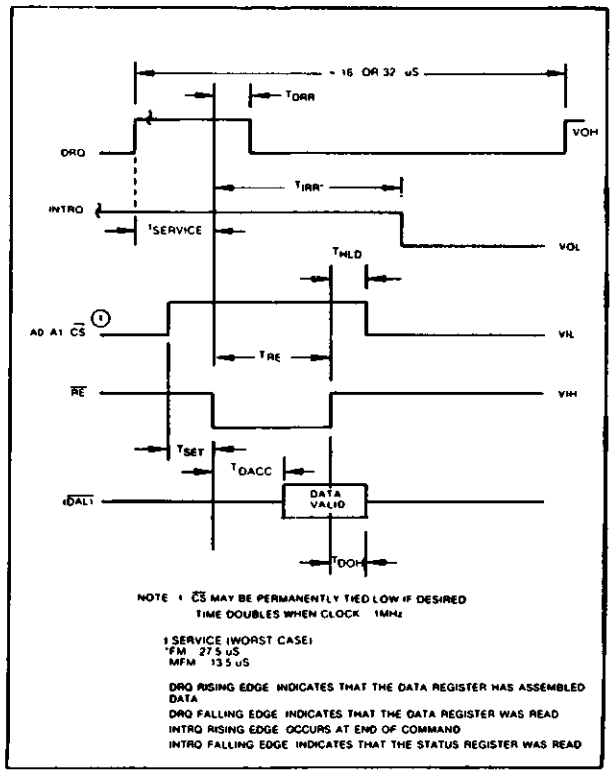
Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 or 1024 bytes.
2) Gap 2 cannot be varied from the IBM format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the FD179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FD179X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.



READ ENABLE TIMING

TIMING CHARACTERISTICS

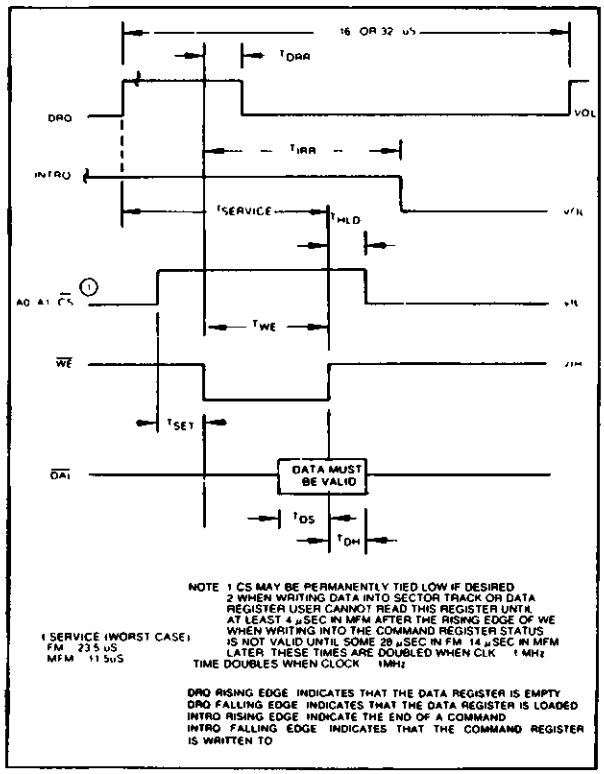
T_A = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING (See Note 6, Page 21)

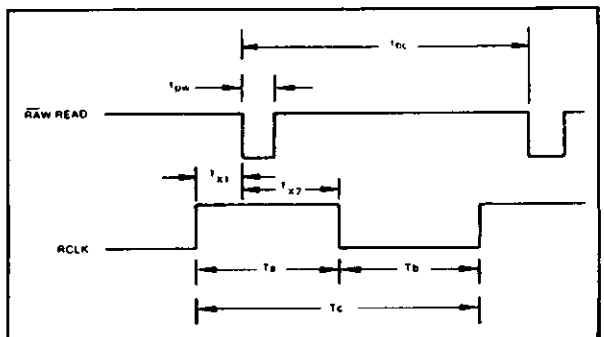
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note 5
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 50 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 50 pf

WRITE ENABLE TIMING (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note 5
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	70			nsec	



WRITE ENABLE TIMING



				NOMINAL		
DISKETTE	MODE	$\overline{DDEN}$	CLK	T_a	T_b	T_c
8"	MFM	0	2 MHz	1 μS	1 μS	2 μS
8"	FM	1	2 MHz	2 μS	2μS	4 μS
5"	MFM	0	1 MHz	2 μS	2μS	4 μS
5"	FM	1	1 MHz	4 μS	4 μS	8 μS

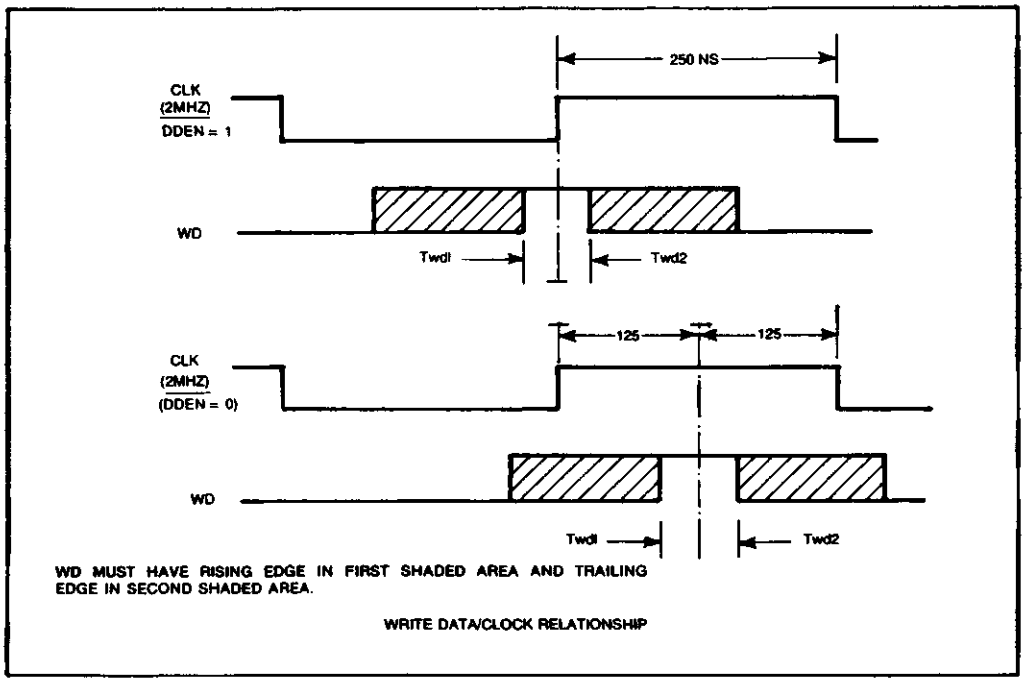
INPUT DATA TIMING

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	See Note 1
tbc	$\overline{\text{Raw Read}}$ Cycle Time	1500	2000		nsec	1800 ns @ 70°C
Tc	RCLK Cycle Time	1500	2000		nsec	1800 ns @ 70°C
Tx_1	RCLK hold to $\overline{\text{Raw Read}}$	40			nsec	See Note 1
Tx_2	$\overline{\text{Raw Read}}$ hold to RCLK	40			nsec	See Note 1

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz) (See Note 6, Page 21)

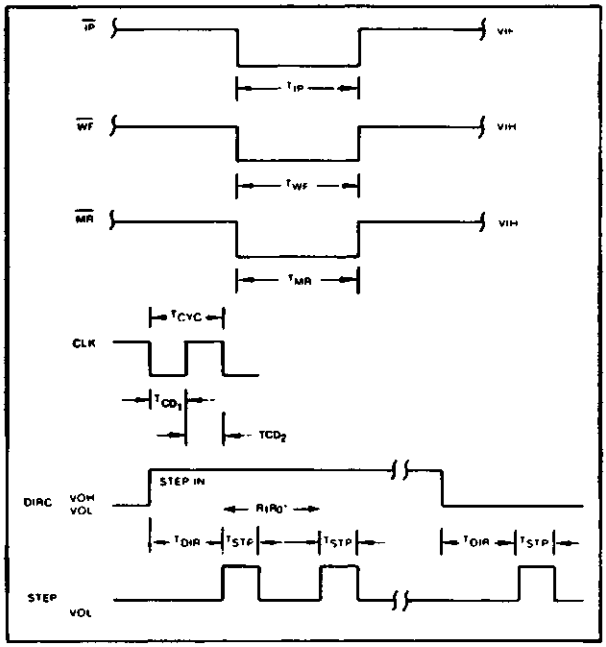
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width		500	650	nsec	FM
			200	350	nsec	MFM
Twg	Write Gate to Write Data		2		μsec	FM
			1		μsec	MFM
Tbc	Write data cycle Time		2,3, or 4		μsec	±CLK Error
Ts	Early (Late) to Write Data	125			nsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM
Twdl	WD Valid to Clk	100			nsec	CLK=1 MHZ
		50			nsec	CLK=2 MHZ
Twd2	WD Valid after CLK	100			nsec	CLK=1 MHZ
		30			nsec	CLK=2 MHZ



WRITE DATA TIMING

MISCELLANEOUS TIMING: (Times Double When Clock = 1 MHz) (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	230	250	20000	nsec	
TCD_2	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			µsec	See Note 5 ± CLK ERROR
TDIR	Dir Setup to Step		12		µsec	
TMR	Master Reset Pulse Width	50			µsec	
TIP	Index Pulse Width	10			µsec	See Note 5
TWF	Write Fault Pulse Width	10			µsec	



MISCELLANEOUS TIMING

*FROM STEP RATE TABLE

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2 μs, nominal in MFM and 4 μs nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during RAW READ (Polarity is unimportant).
5. Times double when clock = 1 MHz.
6. Output timing readings are at V_{OL} = 0.8v and V_{OH} = 2.0v.

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings
- V_{DD} with repect to V_{SS} (ground): + 15 to − 0.3V
- Voltage to any input with respect to V_{SS} = + 15 to − 0.3V
- I_{CC} = 60 MA (35 MA nominal)
- I_{DD} = 15 MA (10 MA nominal)
- C_{IN} & C_{OUT} = 15 pF max with all pins grounded except one under test.
- Operating temperature = 0°C to 70°C
- Storage temperature = − 55°C to + 125°C

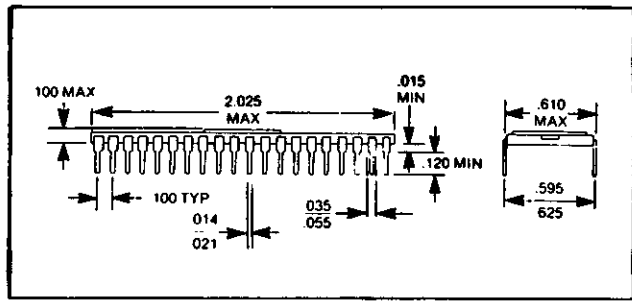
OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = + 5V ± .25V

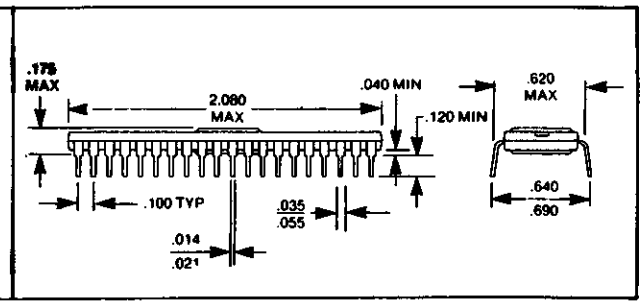
SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{DD}**
I_{OL}	Output Leakage		10	μA	V_{OUT} = V_{DD}
V_{IH}	Input High Voltage	2.6		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.8		V	I_O = − 100 μA
V_{OL}	Output Low Voltage		0.45	V	I_O = 1.6 mA*
P_D	Power Dissipation		0.6	W	

*1792 and 1794 I_O = 1.0 mA

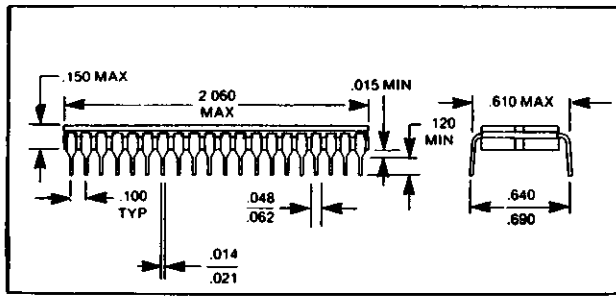
**Leakage conditions are for input pins without internal pull-up resistors. Pins 22, 23, 33, 36, and 37 have pull-up resistors. See Tech Memo #115 for testing procedures.



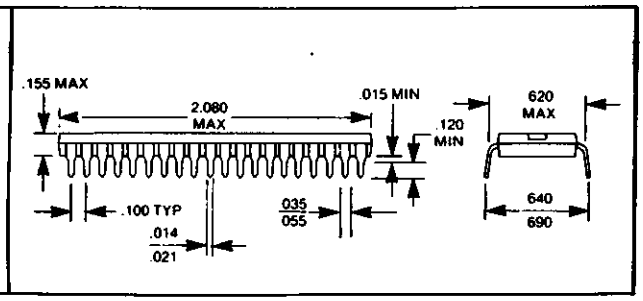
40 LEAD CERAMIC "A" or "AL"



40 LEAD RELPACK "B" or "BL"



40 LEAD CERDIP "CL"



40 LEAD PLASTIC "P" or "PL"

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TECHNICAL MEMO

WESTERN DIGITAL
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MEMO: 169

DEVICE: WD1770/1772/1773

TITLE: Preliminary Data Sheet Update

DATE: 8/29/83

The following information represents updates to the current WD1770/72/73 Preliminary Data sheet. These updates are performance enhancements.

1. TRE (Page 19) Changed from MIN 150NS to MIN 200NS.

2. TAH (Page 19) Changed from MIN 20NS to 10NS.

3. TWE (Page 19) Changed from MIN 150NS to MIN 200NS.

4. H bit in Command (Page 6 last paragraph)
   Changed from: "If the hFlag is set and motor on line (Pin 20)"

   Changed to: "If the hFlag is NOT set and motor on line (Pin 20)"

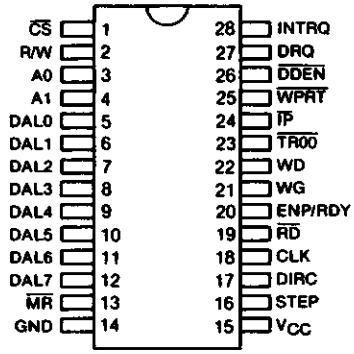
WESTERN DIGITAL
CORPORATION

PRELIMINARY

WD1773 5¼" Floppy Disk Controller/Formatter

FEATURES

- 100% SOFTWARE COMPATIBILITY WITH WD1793
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- SINGLE (FM) AND DOUBLE (MFM) DENSITY
- 28 PIN DIP, SINGLE +5V SUPPLY
- TTL COMPATIBLE INPUTS/OUTPUTS
- 128, 256, 512 OR 1024 SECTOR LENGTHS
- 8-BIT BI-DIRECTIONAL HOST INTERFACE



PIN DESIGNATION

DESCRIPTION

The WD1773 is an MOS/LSI device which performs the functions of a 5¼" Floppy Disk Controller/ Formatter. It is fully software compatible with the Western Digital WD1793-02, allowing the designer to reduce parts count and board size on an existing WD1793 based design without software modifications.

With the exception of the enable Precomp/Ready line, the WD1773 is identical to the WD1770 controller. This line serves as both a READY input from the drive during READ/STEP operations, and as a Write Precompensation enable during Write operations. A built-in digital data separator virtually eliminates all external components associated with data recovery in previous designs.

The WD1773 is implemented in NMOS silicon gate technology and is available in a 28 pin, dual-in-line package.

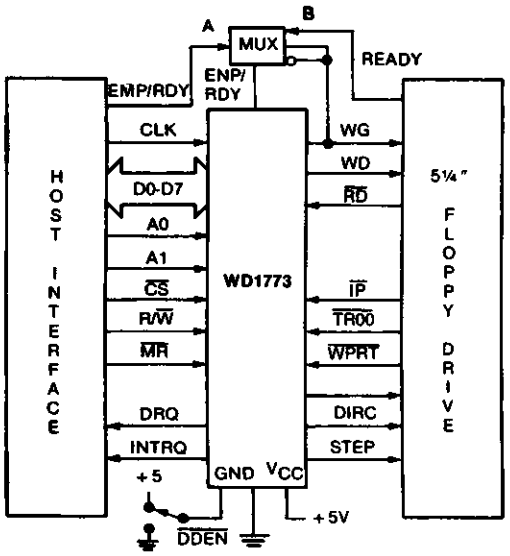
January, 1984

PIN DESCRIPTION

PIN NUMBER	PIN NAME	MNEMONIC	FUNCTION
1	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enable Host communication with the device.
2	READ/WRITE	R/$\overline{W}$	A logic high on this input controls the placement of data on the $\overline{D0}$-$\overline{D7}$ lines from a selected register, while a logic low causes a write operation to a selected register.
3,4	ADDRESS 0,1	A0, A1	These two inputs select a register to Read/Write data: $\overline{CS}$ A1 A0 R/$\overline{W}$ = 1 R/$\overline{W}$ = 0 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
5-12	DATA ACCESS LINES 0 THROUGH 7	DAL0-DAL7	Eight bit bidirectional bus used for transfer of data, control, or status. This bus is enabled by $\overline{CS}$ and R/$\overline{W}$. Each line will drive one TTL load.
13	MASTER RESET	$\overline{MR}$	A logic low pulse on this line resets the device and initializes the status register. Internal pull-up.
14	GROUND	GND	Ground.
15	POWER SUPPLY	V_{CC}	+5V ±5% power supply input.
16	STEP	STEP	The Step output contains a pulse for each step of the drive's R/$\overline{W}$ head.
17	DIRECTION	DIRC	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
18	CLOCK	CLK	This input requires a free-running 40 to 60% duty cycle clock (for internal timing) at 8 MHZ ±1%.
19	READ DATA	$\overline{RD}$	This active low input is the raw data line containing both clock and data pulses from the drive.
20	ENABLE PRECOMP/ READY LINE	ENP/RDY	Serves as a READY input from the drive during READ/STEP operations and as a Write Precomp enable during write operations.
21	WRITE GATE	WG	This output is made valid prior to writing on the diskette.
22	WRITE DATA	WD	FM or MFM clock and data pulses are placed on this line to be written on the diskette.
23	TRACK 00	$\overline{TR00}$	This active low input informs the WD1773 that the drive's R/$\overline{W}$ heads are positioned over Track zero.
24	INDEX PULSE	$\overline{IP}$	This active low input informs the WD1773 when the physical index hole has been encountered on the diskette.
25	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing. Internal pull-up.
26	DOUBLE DENSITY ENABLE	$\overline{DDEN}$	This input pin selects either single (FM) or double (MFM) density. When $\overline{DDEN}$ = 0, double density is selected. Internal pull-up.

PIN DESCRIPTION (CONTINUED)

PIN NUMBER	PIN NAME	MNEMONIC	FUNCTION
27	DATA REQUEST	DRQ	This active high output indicates that the Data Register is full (on a Read) or empty (on a Write operation).
28	INTERRUPT REQUEST	INTRQ	This active high output is set at the completion of any command or reset a read of the Status Register.



WD1773 SYSTEM BLOCK DIAGRAM

ARCHITECTURE

The Floppy Disk Formatter block diagram is illustrated on page 4. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (RD) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

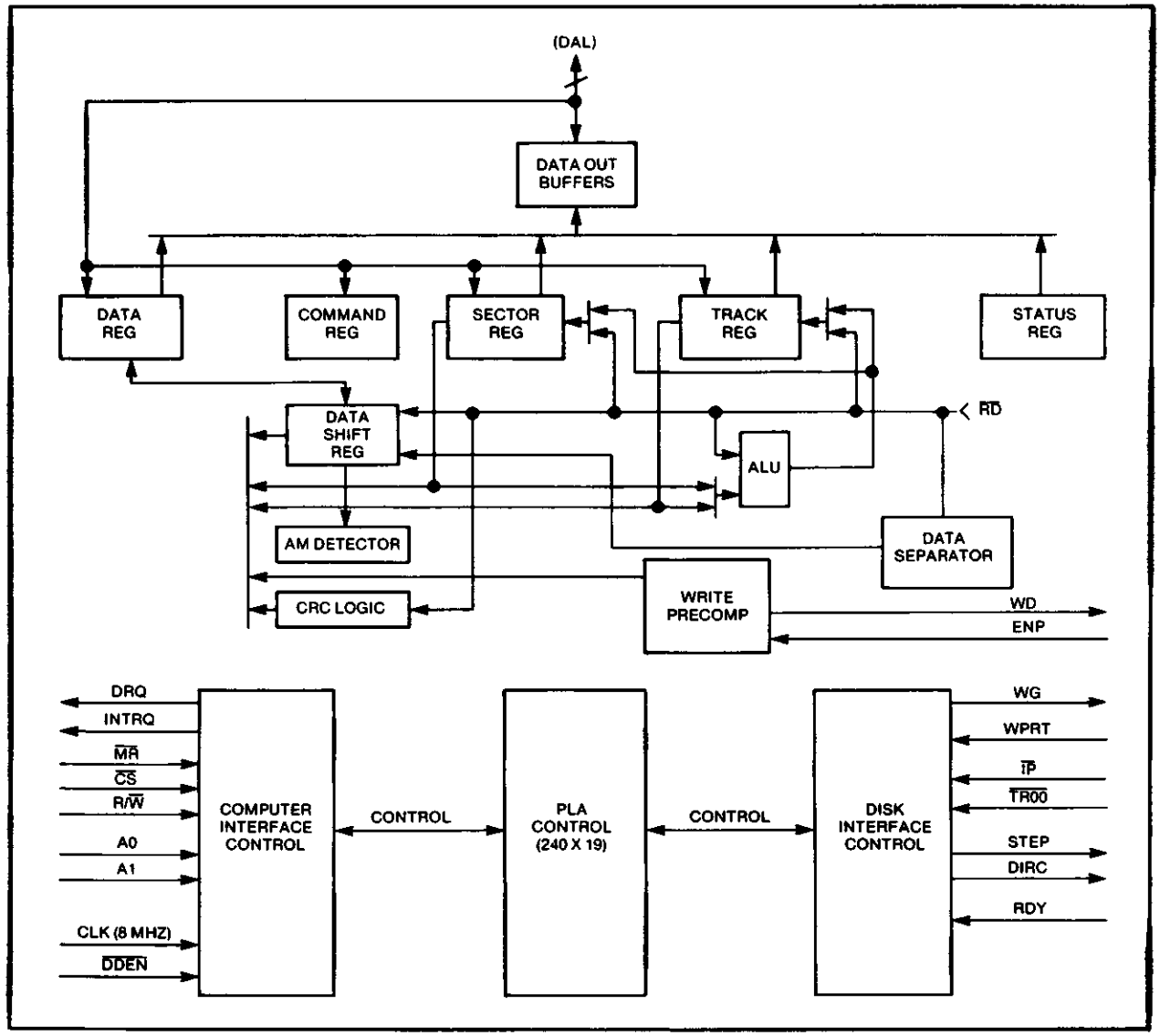
Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is:
$G(x) = x^{16} + x^{12} + x^5 + 1$.
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.



WD1773 BLOCK DIAGRAM

Timing and Control — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock. The WD1773 has two different modes of operation according to the state of DDEN. When DDEN = 0, double density (MFM) is enabled. When DDEN = 1, single density is enabled.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

Data Separator — A digital data separator consisting of a ring shift register and data window detection logic provides read data and a recovery clock to the AM detector.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD1773. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and R/W = 1 are active or act as input receivers when CS and R/W = 0 are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The address bits A1 and A0, combined with the signal R/W during a Read operation or Write operation are interpreted as selecting the following registers:

A1	A0	READ (R/W = 1)	WRITE (R/W = 0)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD1773 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operations continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The WD1773 has two modes of operation according to the state DDEN (Pin 26). When DDEN = 1, single density is selected. In either case, the CLK input (Pin 18) is at 8 MHZ.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, DDEN should be placed to logical "1." For MFM formats, DDEN should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

SECTOR LENGTH TABLE	
SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
00	128
01	256
02	512
03	1024

The number of sectors per tract as far as the WD1773 is concerned can be from 1 to 255 sectors. The number of tracks as far as the WD1773 is concerned is from 0 to 255 tracks.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the device before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For Write operations, the WD1773 provides Write Gate (Pin 21) to enable a Write condition, and Write Data (Pin 22) which consists of a series of active high pulses. These pulses contain both Clock and Data information in FM and MFM. Write Data provides the unique missing clock patterns for recording Address Marks.

If Precomp Enable (ENP) is active when WG is asserted, automatic Write Precompensation takes place. The outgoing Write Data stream is delayed or advanced from nominal by 125 nanoseconds according to the following table:

PATTERN				MFM	FM
X	1	1	0	Early	N/A
X	0	1	1	Late	N/A
0	0	0	1	Early	N/A
1	0	0	0	Late	N/A

Next Bit to be sent
Current Bit sending
Previous Bits sent

Precompensation is typically enabled on the innermost tracks where bit shifts usually occur and bit density is at its maximun.

COMMAND DESCRIPTION

The WD1773 will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

COMMAND TYPE	BIT NO(S)		DESCRIPTION
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Don't Care	
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No 30 MS delay E = 1, 15 MS delay
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	

	LSB's Sector Length in ID Field 00	01	10	11
L = 0	256	512	1024	128
L = 1	128	256	512	1024

II	4	m = Multiple Record Flag — m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset I_3-I_1 = 0 Terminate With No Interrupt (INTRQ)

*NOTE: See Type IV Command Description for further information.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0 r_1), which determines the stepping motor rate as defined in Table 3.

A 4 μs (MFM) or 8 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 24 or 48 μsec before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by settling bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 30 msec settling time. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The WD1773 must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the r_1 r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the WD1773 terminates operation, interrupts, and sets the Seek error status bit, providing the V flag is set. A verification operation also takes place if the V flag is set. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state and that the DRQ pin stays low.

SEEK

This command assumes that the Track Register contains the track number of he current position of the Read-Write head and the Data Register contains the desired track number. The WD1773 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the WD1773 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the WD1773 issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. An interrupt is generated at the completion of the command.

STEP-OUT

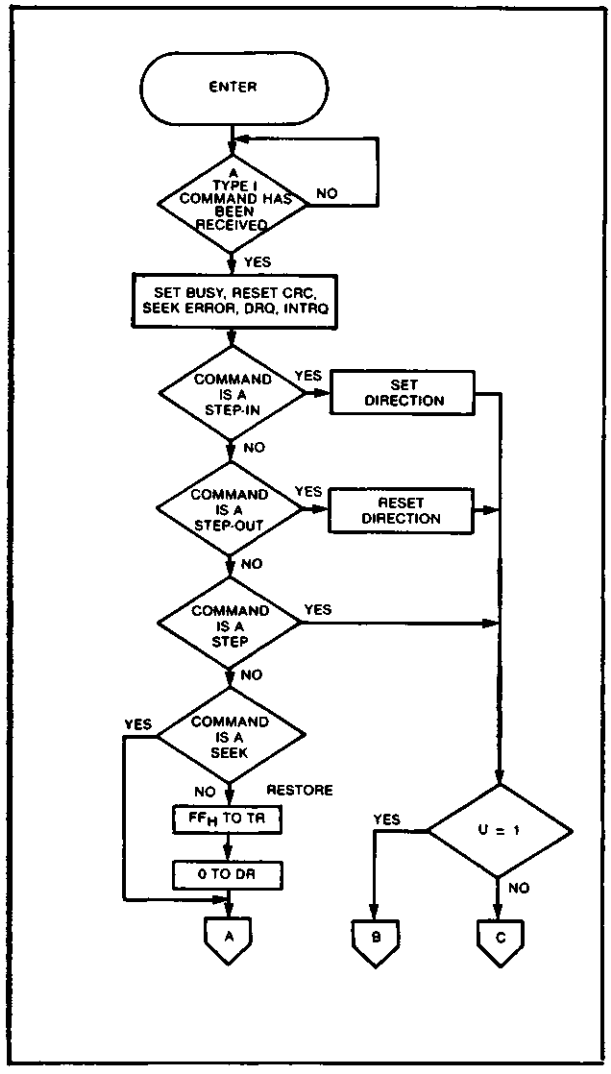
Upon receipt of this command, the WD1773 issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

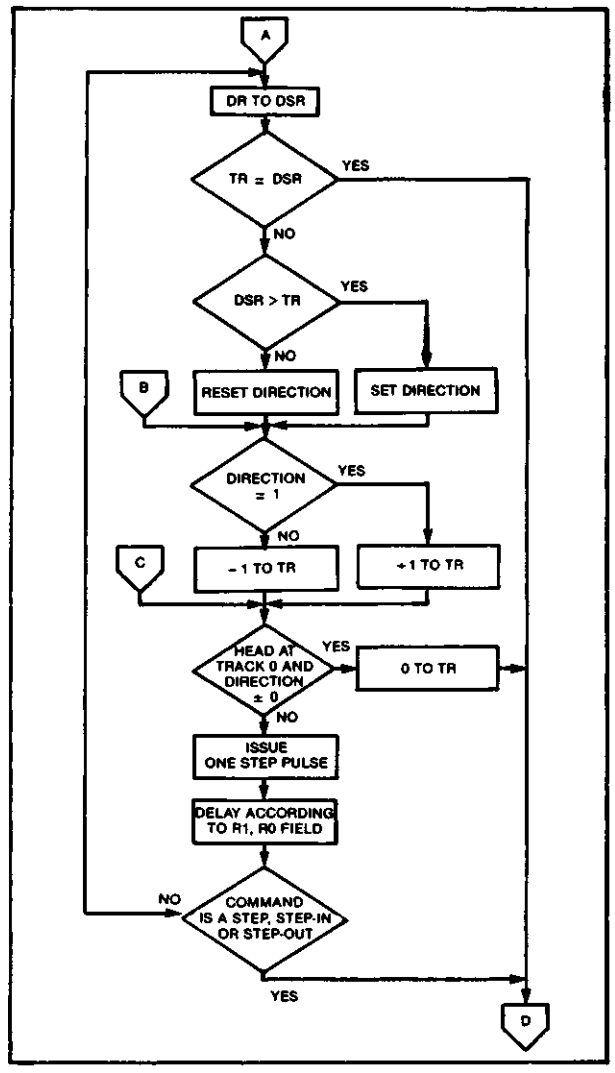
The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. The E flag is still active providing a delay of 1 to 30 msec for head settling time.

When an ID field is located on the disk, the WD1773 compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The WD1773 must find an ID field with a Track number, Sector number, side number, and CRC within five revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an inter-



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

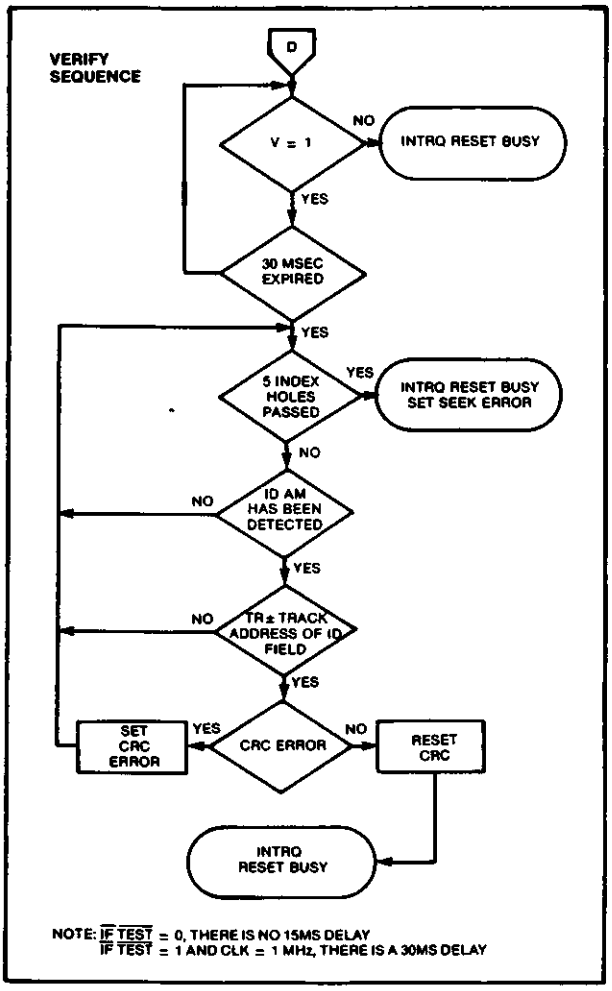
rupt is generated at the completion of the command. if m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The WD1773 will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the WD1773 is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The WD1773 will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for WD1773 contain side compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the WD1773 continues with the ID search. If a comparison is not made within 6 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

READ SECTOR

Upon receipt of the Read Sector command, the Busy status bit is set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field is searched for and verified again followed by the Data Address Mark search. If after 5 revolutions the DAM cannot be found, the Record Not Found status bit is set and the operation is terminated.



TYPE I COMMAND FLOW

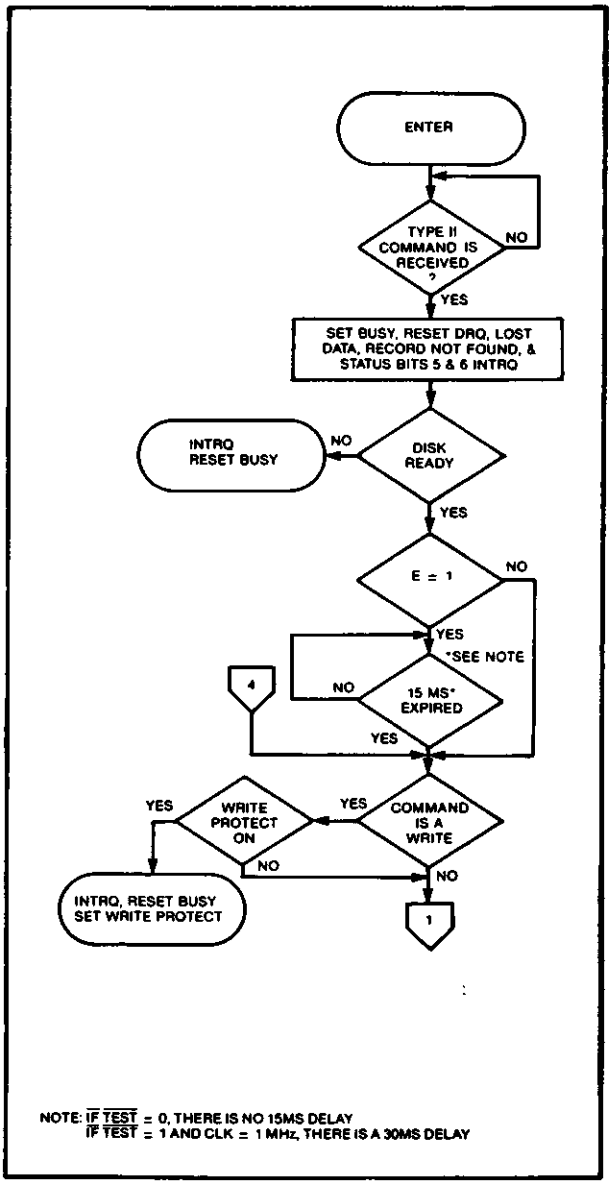
When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete dta field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The WD1773 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by



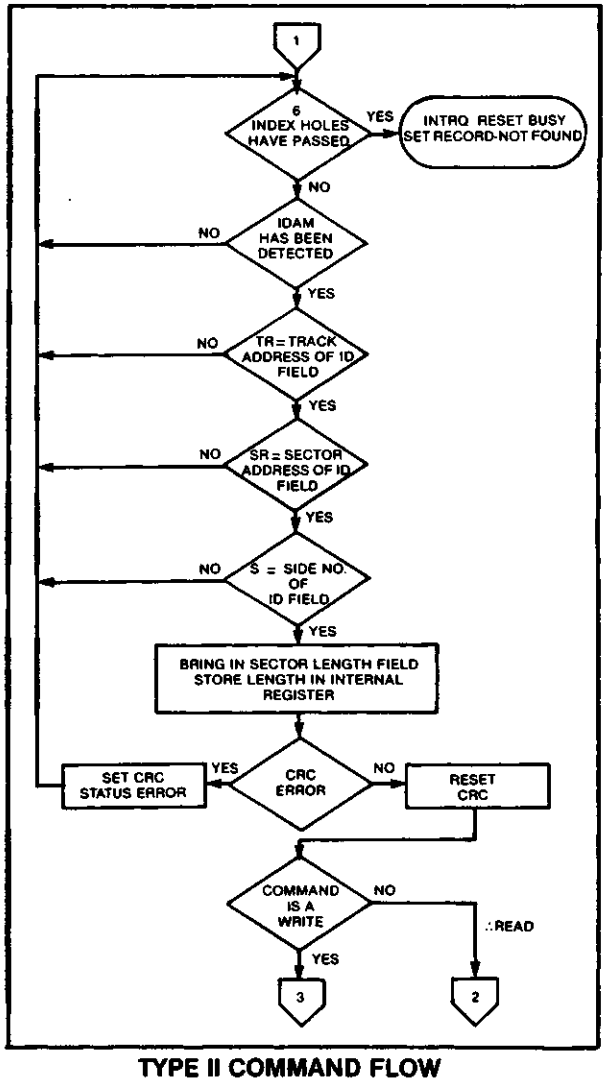
TYPE II COMMAND FLOW

the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on

the disk as determined by the a0 field of the command as shown below:

a0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The WD1773 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. The INTRQ will set 48 μsec (MFM) or 96 μsec (FM) after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.



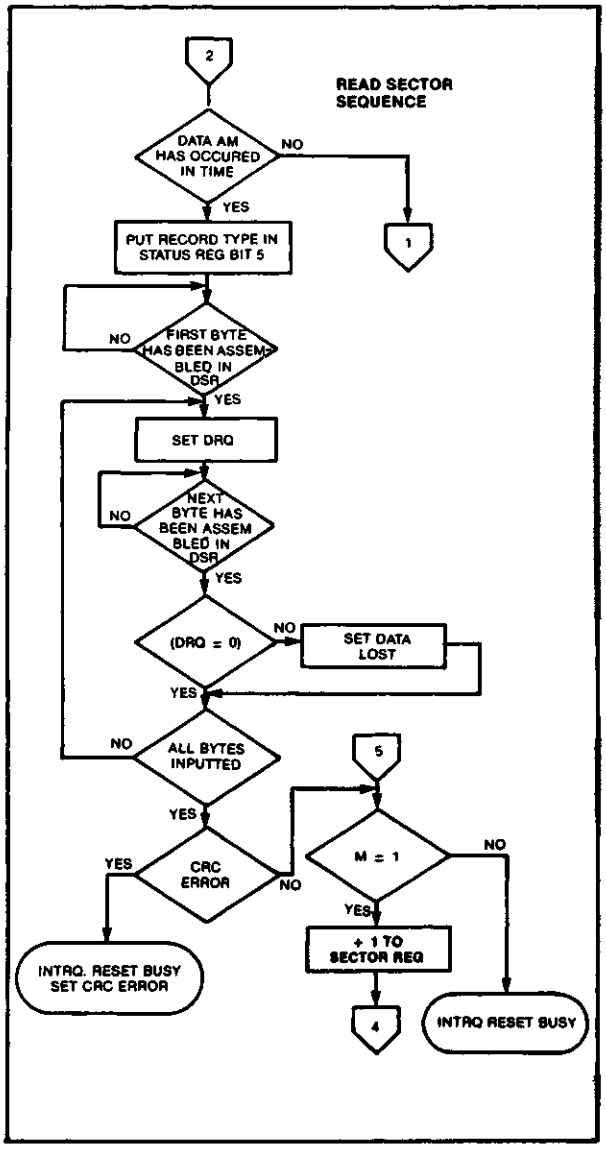
TYPE II COMMAND FLOW

TYPE III COMMANDS

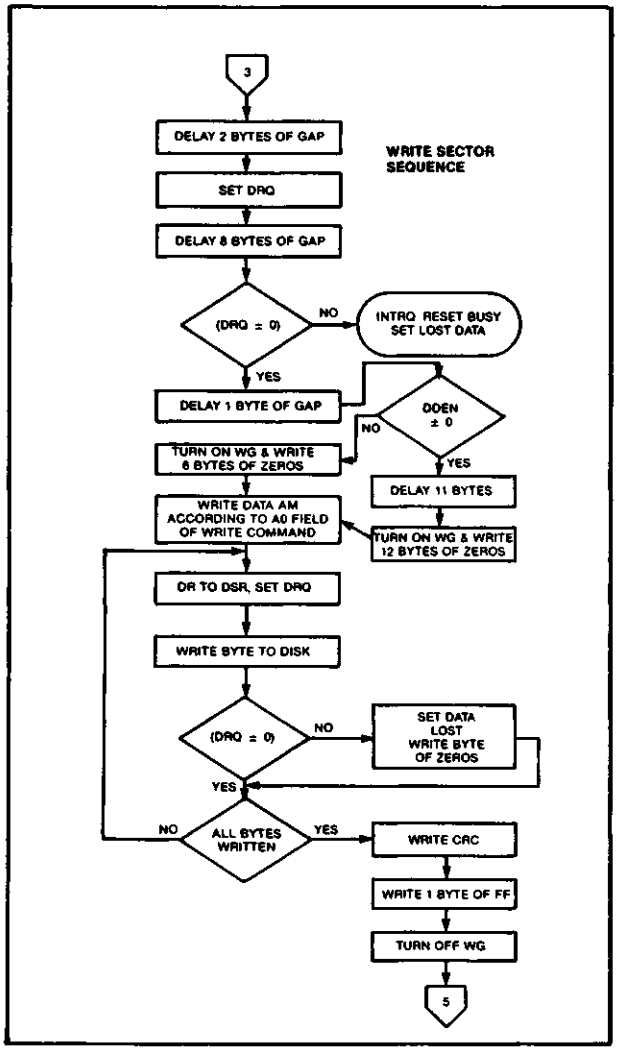
READ ADDRESS

Upon receipt of the Read Address command, the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6



TYPE II COMMAND FLOW



TYPE II COMMAND

Although the CRC characters are transferred to the computer, the WD1773 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

Upon receipt of the READ track command, the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the WD1773 detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be tranferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

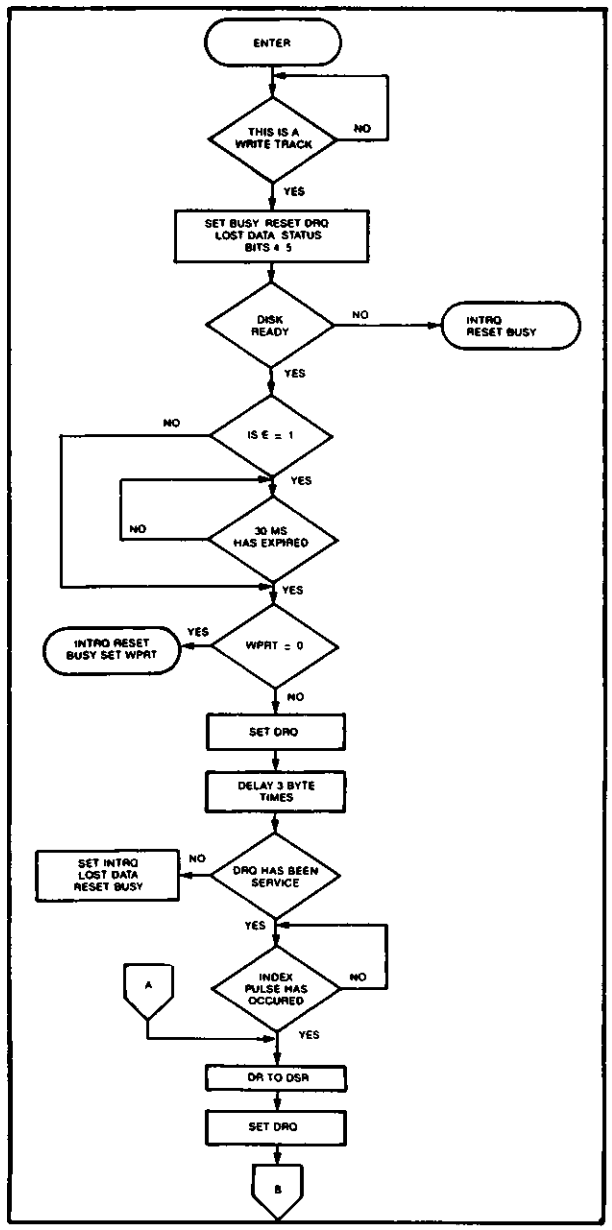
The Forced Interrupt command is generally used to

terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

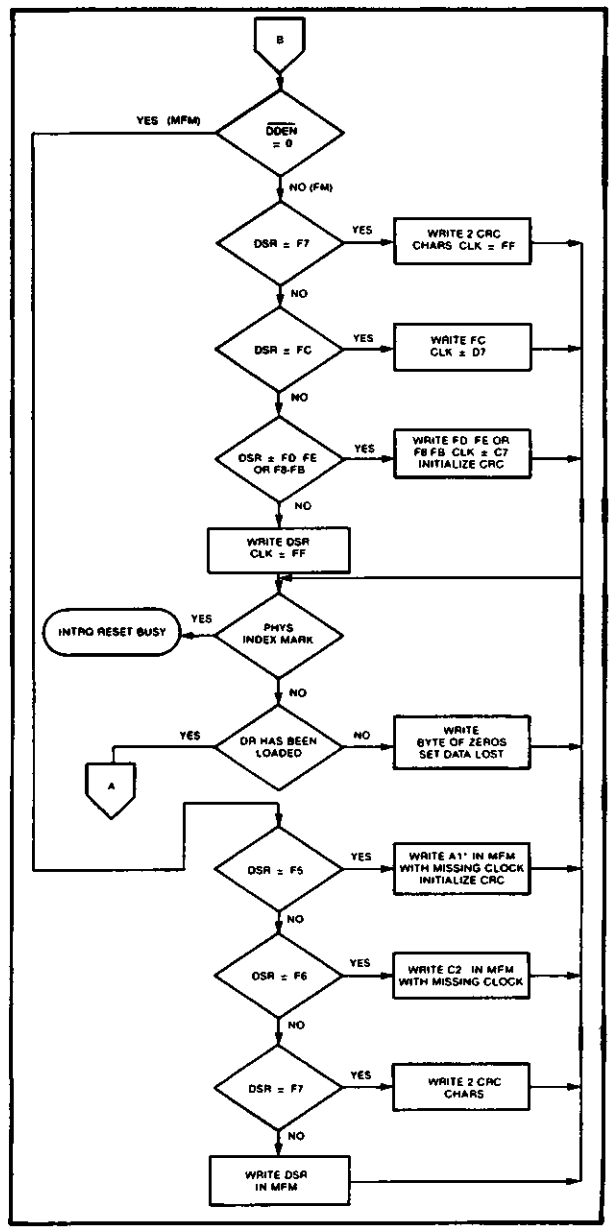
The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 16 μsec (double density) or 32 μsec (single density before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	48 μs	24 μs
Write to Command Reg.	Read Status Bits 1-7	64 μs	32 μs
Write Register	Read Any Register	32 μs	16 μs

IBM 3740 FORMAT — 128 BYTES/SECTOR

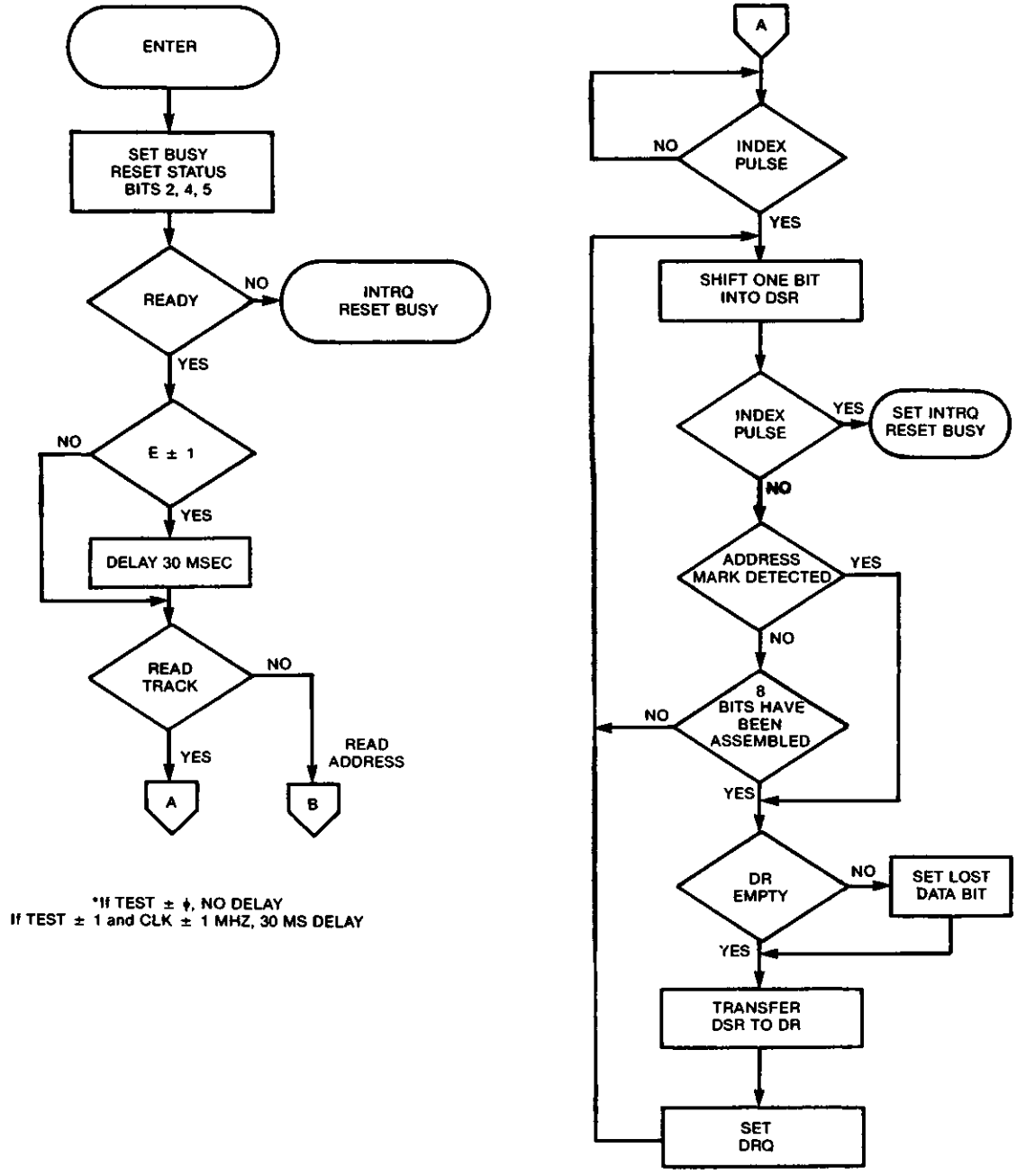
Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)'
6	00
1	FC (Index Mark)
26	FF (or 00)'
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)'
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)'
247**	FF (or 00)'

*Write bracketed field 26 times
**Continue writing until WD1773 interrupts out. Approx. 247 bytes.

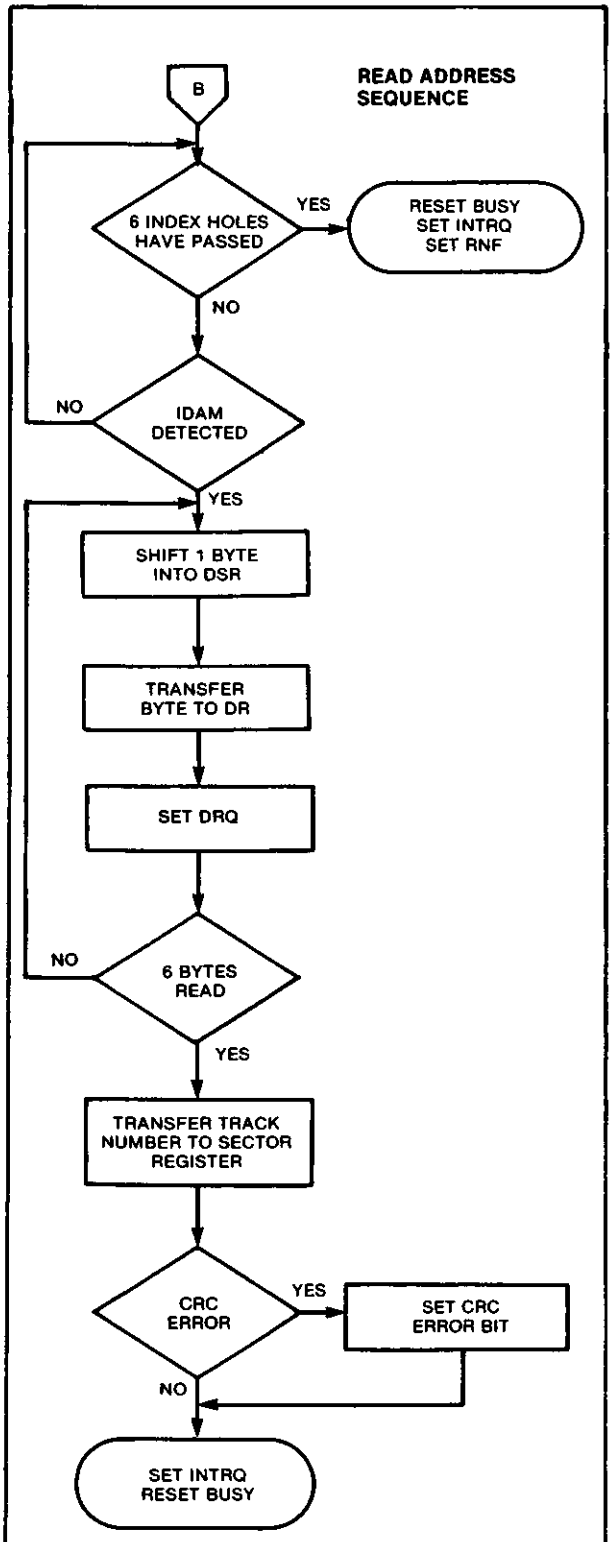
IBM SYSTEM 34 FORMAT — 256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.



*If TEST ± ϕ, NO DELAY
If TEST ± 1 and CLK ± 1 MHZ, 30 MS DELAY

TYPE III COMMAND
Read Track/Address



TYPE III COMMAND
Read Track/Address

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
* 50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

*Write bracketed field 26 times
**Continue writing until WD1773 interrupts out. Approx. 598 bytes.

1. NON-IBM FORMATS

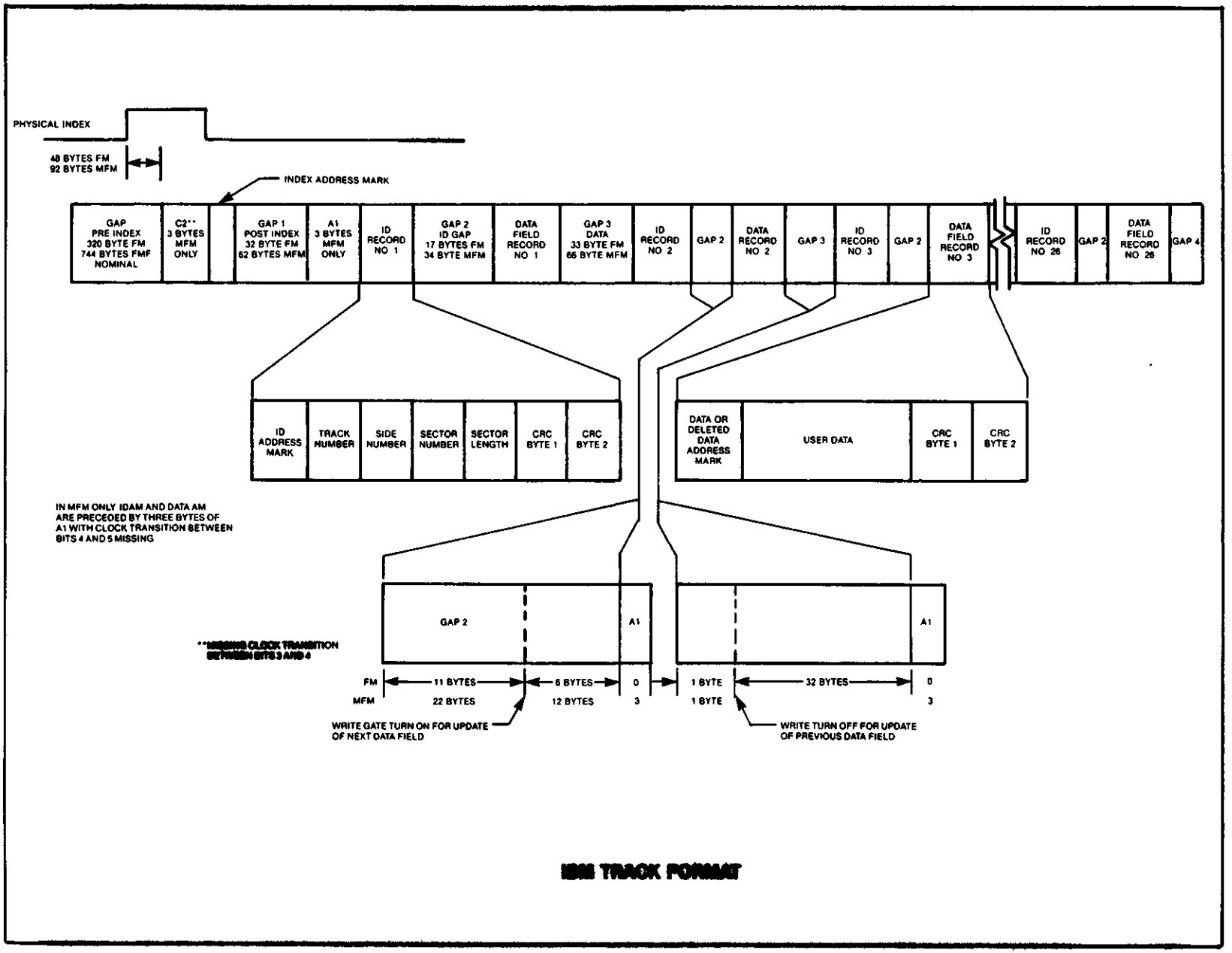
Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.
2) Gap 2 cannot be varied from the IBM format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation. Gap 1, 3, and 4 lengths can be as short as 2 bytes, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.



IBM TRACK FORMAT

DC ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to 70°C Ambient

Maximum Voltage to Any Input with Respect to V_{SS} ..... (−15 to −0.3V)

DC OPERATING CHARACTERISTICS

TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ±.25V

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	$I_0 = -100\mu A$
V_{OL}	Output Low Voltage		0.40	V	$I_0 = 1.6$ mA
P_D	Power Dissipation		.75	W	
R_{PU}	Internal Pull-Up	100	1700	μA	$V_{IN} = 0V$
I_{CC}	Supply Current	75 (Typ)	150	mA	

AC TIMING CHARACTERISTICS

TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ±.25V

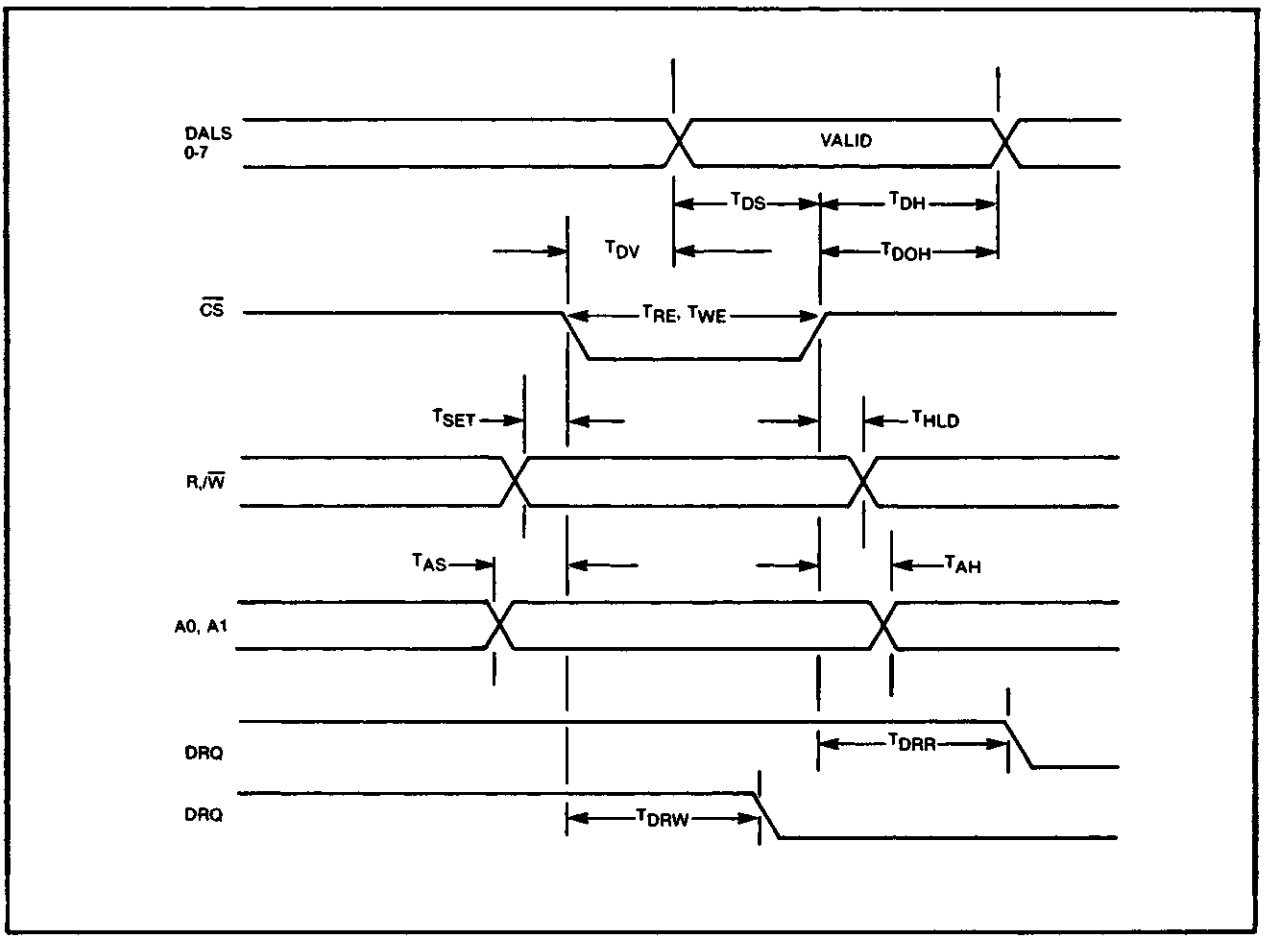
READ ENABLE TIMING — RE such that: R/W = 1, CS = 0.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TRE	RE Pulse Width of $\overline{CS}$	200			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		25	100	nsec	
TIRR	INTRQ Reset from $\overline{RE}$			8000	nsec	
TDV	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
TDOH	Data Hold from $\overline{RE}$	50		150	nsec	C_L = 50 pf

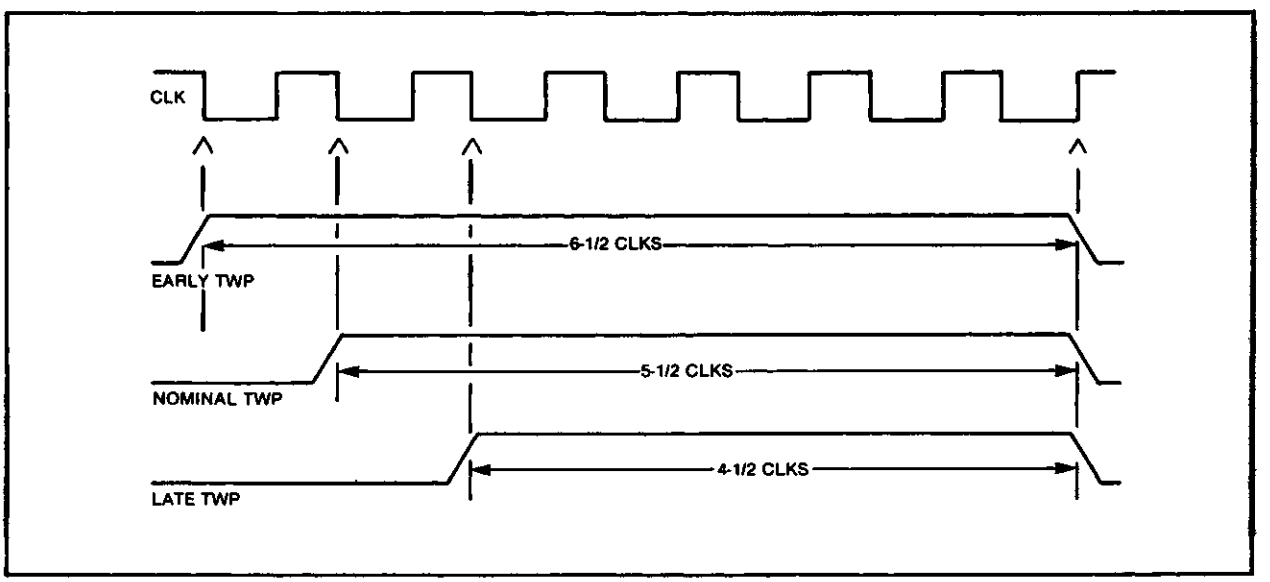
Note: DRQ and INTRQ reset are from rising edge (lagging) of RE, whereas resets are from falling edge (leading) of WE.

WRITE ENABLE TIMING — WE such that: R/W = 0, CS = 0.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TAS	Setup ADDR to $\overline{CS}$	50			nsec	
TSET	Setup R/$\overline{W}$ to $\overline{CS}$	0			nsec	
TAH	Hold ADDR from $\overline{CS}$	10			nsec	
THLD	Hold R/$\overline{W}$ from $\overline{CS}$	0			nsec	
TWE	$\overline{WE}$ Pulse Width	200			nsec	
TDRW	DRQ Reset from $\overline{WE}$		100	200	nsec	
TIRW	INTRQ Reset from $\overline{WE}$			8000	nsec	
TDS	Data Setup to $\overline{WE}$	150			nsec	
TDH	Data Hold from $\overline{WE}$	0			nsec	



REGISTER TIMINGS



WRITE DATA TIMING

WRITE DATA TIMING:

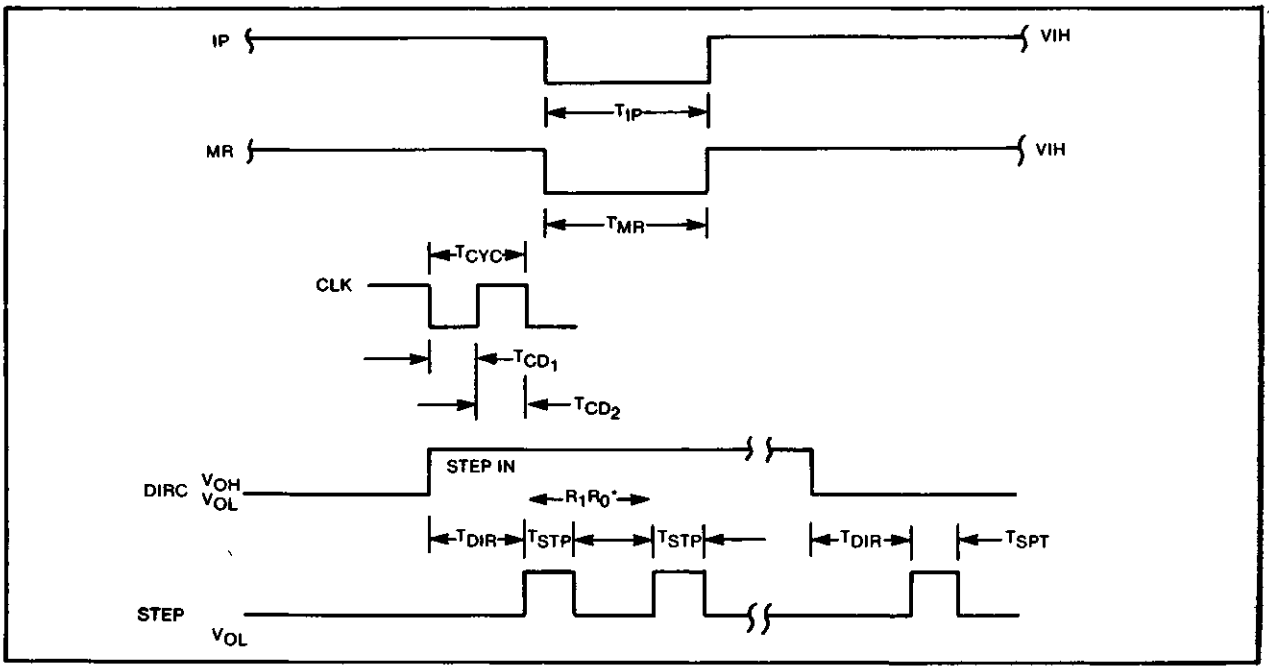
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TWG	Write Gate to Write Data		4 2		µsec µsec	FM MFM
TBC	Write Data Cycle Time		4,6,8		µsec	
TWF	Write Gate off from WD		4 2		µsec µsec	FM MFM
TWP	Write Data Pulse Width		820 690 570 1380		nsec nsec nsec nsec	Early MFM Nominal MFM Late MFM FM

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TPW	Raw Read Pulse Width	200		3000	nsec	
TBC	Raw Read Cycle Time	3000			nsec	

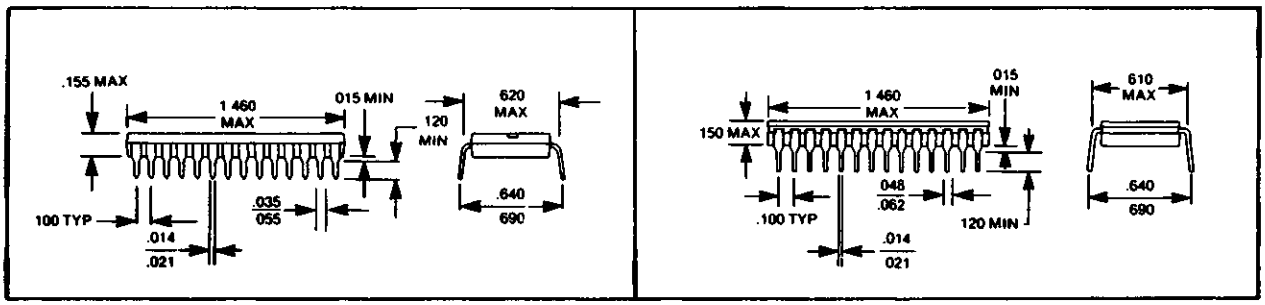
MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	50	67		nsec	(60/40)
TCD_2	Clock Duty (high)	50	67		nsec	(40/60)
TSTP	Step Pulse Output		4 8		µsec	MFM FM
TDIR	Dir Setup to Step		24 48		µsec	MFM FM
TMR	Master Reset Pulse Width	50			µsec	
TIP	Index Pulse Width	20			µsec	



MISCELLANEOUS TIMING

Package Diagrams



28 LEAD PLASTIC "R" or "PH"

28 LEAD CERDIP "CH"

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WESTERN DIGITAL
CORPORATION

WD9216-00/WD9216-01
Floppy Disk Data Separator — FDDS

FEATURES

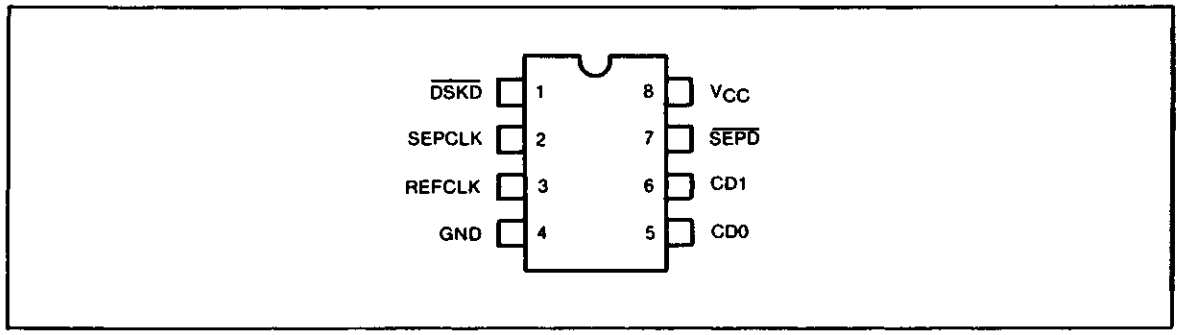
- PERFORMS COMPLETE DATA SEPARATION FUNCTION FOR FLOPPY DISK DRIVES
- SEPARATES FM OR MFM ENCODED DATA FROM ANY MAGNETIC MEDIA
- ELIMINATES SEVERAL SSI AND MSI DEVICES NORMALLY USED FOR DATA SEPARATION
- NO CRITICAL ADJUSTMENTS REQUIRED
- COMPATIBLE WITH WESTERN DIGITAL 179X, 176X AND OTHER FLOPPY DISK CONTROLLERS
- SMALL 8-PIN DUAL-IN-LINE PACKAGE
- +5 VOLT ONLY POWER SUPPLY
- TTL COMPATIBLE INPUTS AND OUTPUTS

GENERAL DESCRIPTION

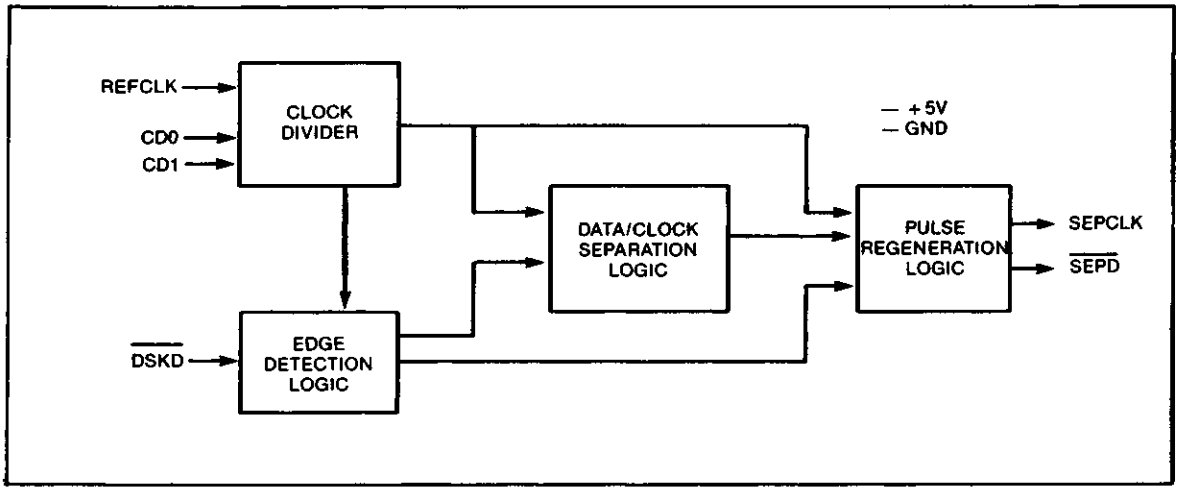
The Floppy Disk Data Separator provides a low cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate Clock and Data inputs for a Floppy Disk Controller.

The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and reclocking circuitry. Supplied in an 8-pin Dual-In-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL compatible on all inputs and outputs.

The WD9216 is available in two versions; the WD9216-00, which is intended for 5¼" disks and the WD9216-01 for 5¼" and 8" disks.



PIN CONFIGURATION



FLOPPY DISK DATA SEPARATOR BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −55°C to 125°C
Positive Voltage on any Pin,
with respect to ground . . . . . +8.0V
Negative Voltage on any Pin,
with respect to ground . . . . . −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

OPERATING CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, unless otherwise noted)

PARAMETER		MIN.	TYP.	MAX.	UNITS	COMMENTS
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level V_{IL}				0.8	V	
High Level V_{IH}		2.0			V	
OUTPUT VOLTAGE LEVELS						
Low Level V_{OL}				0.4	V	I_{OL} = 1.6mA
High Level V_{OH}		2.4			V	I_{OH} = −100μA
INPUT CURRENT						
Leakage I_{IL}				10	μA	$0 \leq V_{IN} \leq V_{DD}$
INPUT CAPACITANCE						
All Inputs				10	pF	
POWER SUPPLY CURRENT						
I_{DD}				50	mA	
A.C. CHARACTERISTICS						
Symbol						
f_{CY}	REFCLK Frequency	0.2		4.3	MHz	WD 9216-00
f_{CY}	REFCLK Frequency	0.2		8.3	MHz	WD 9216-01
t_{CKH}	REFCLK High Time	50		2500	ns	
t_{CKL}	REFCLK Low Time	50		2500	ns	
t_{SDON}	REFCLK to $\overline{SEPD}$ "ON" Delay		100		ns	
t_{SDOFF}	REFCLK to $\overline{SEPD}$ "OFF" Delay		100		ns	
t_{SPCK}	REFCLK to SEPCLK Delay	100			ns	
t_{DLL}	DSKD Active Low Time	0.1		100	μs	
t_{DLH}	DSKD Active High Time	0.2		100	μs	

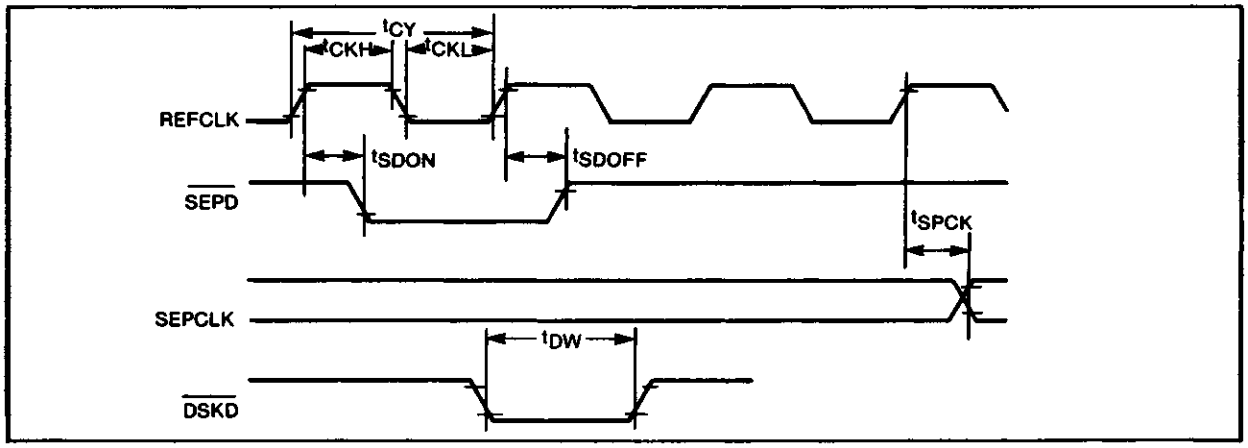


Figure 3. AC CHARACTERISTICS

DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	$\overline{\text{Disk Data}}$	$\overline{\text{DSKD}}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference clock input.
4	Ground	GND	Ground.
5,6	Clock Divisor	CD0, CD1	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: **CD1** CD0 Divisor **0** 0 1 **0** 1 2 1 0 4 1 1 8
7	$\overline{\text{Separated Data}}$	$\overline{\text{SEPD}}$	SEPD is the data output of the FDDS
8	Power Supply	V_{CC}	+5 volt power supply

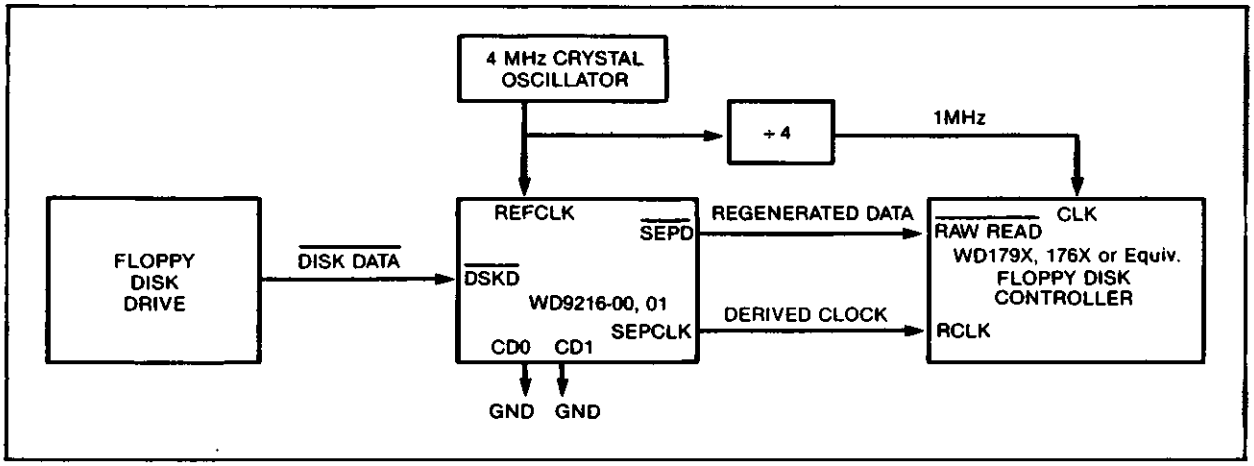


Figure 1.
TYPICAL SYSTEM CONFIGURATION
(5¼" Drive, Double Density)

OPERATION

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

TABLE 1:
CLOCK DIVIDER SELECTION TABLE

DRIVE (8" or 5¼")	DENSITY (DD or SD)	REFCLK MHz	CD1	CD0	REMARKS
8	DD	8	0	0	Select either one
8	SD	8	0	1	
8	SD	4	0	0	
5¼	DD	8	0	1	Select either one
5¼	DD	4	0	0	
5¼	SD	8	1	0	Select any one
5¼	SD	4	0	1	
5¼	SD	2	0	0	

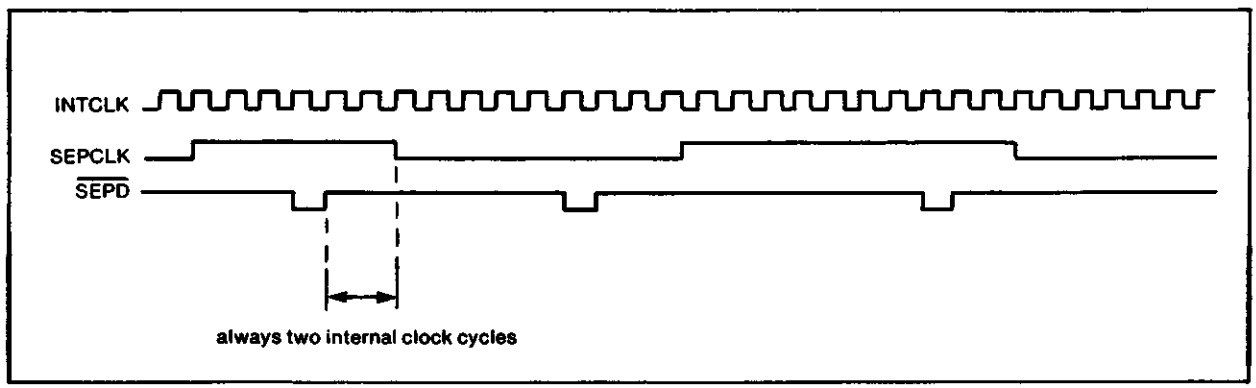


Figure 2.

See page 725 for ordering information.

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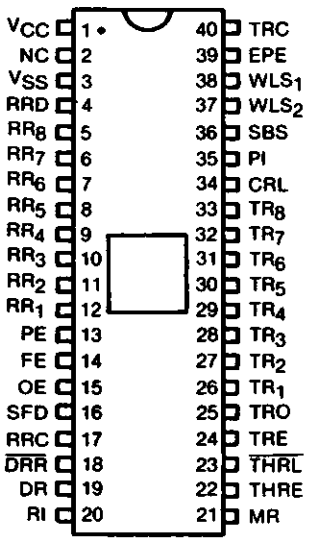
WESTERN DIGITAL
CORPORATION

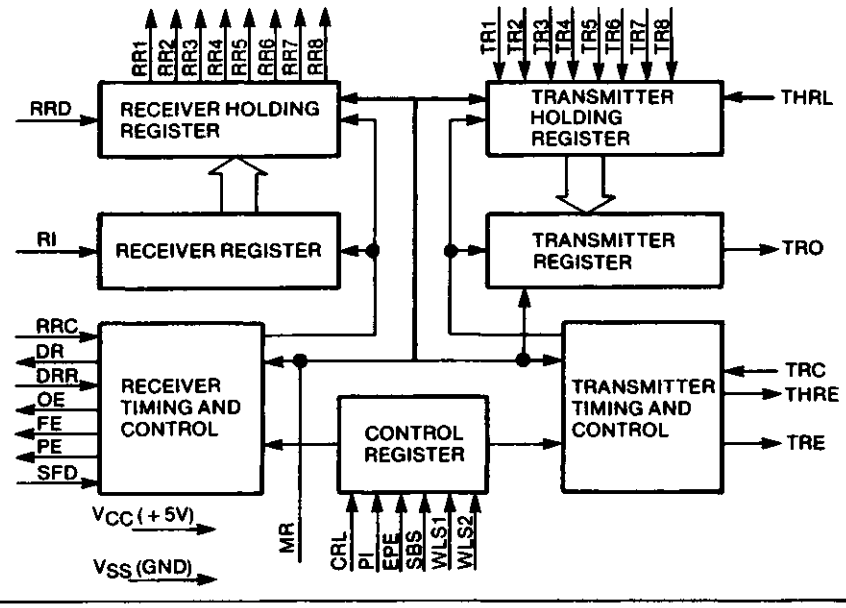
TR1863/TR1865
Universal Asynchronous Receiver/Transmitter (UART)

FEATURES
- SINGLE POWER SUPPLY — +5VDC
- D.C. TO 1 MHZ (64 KB) (STANDARD PART) TR1863/5
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  Parity Inhibit
  One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- TTL COMPATIBLE
- TR1865 HAS PULL-UP RESISTORS ON ALL INPUTS

APPLICATIONS
- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES



PIN CONNECTIONS



TR1863/TR1865 BLOCK DIAGRAM

GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UART) is a general purpose, programmable or hardwired MOS/LSI device. The UART is used to convert parallel data to a serial data format on the transmit side, and converts a serial data format to parallel data on the receive side.

The serial format in order of transmission and reception is a start bit, followed by five to eight data bits, a parity bit (if selected) and one, one and one-half, or two stop bits.

Three types of error conditions are available on each received character: parity error, framing error (no valid stop bit) and overrun error.

The transmitter and receiver operate on external 16X clocks, where 16 clock times are equal to one bit time. The receiver clock is also used to sample in the center of the serial data bits to allow for line distortion.

Both transmitter and receiver are double buffered allowing a one character time maximum between a data read or write. Independent handshake lines for receiver and transmitter are also included. All inputs and outputs are TTL compatible with three-state outputs available on the receiver, and error flags for bussing multiple devices.

PIN DEFINITIONS

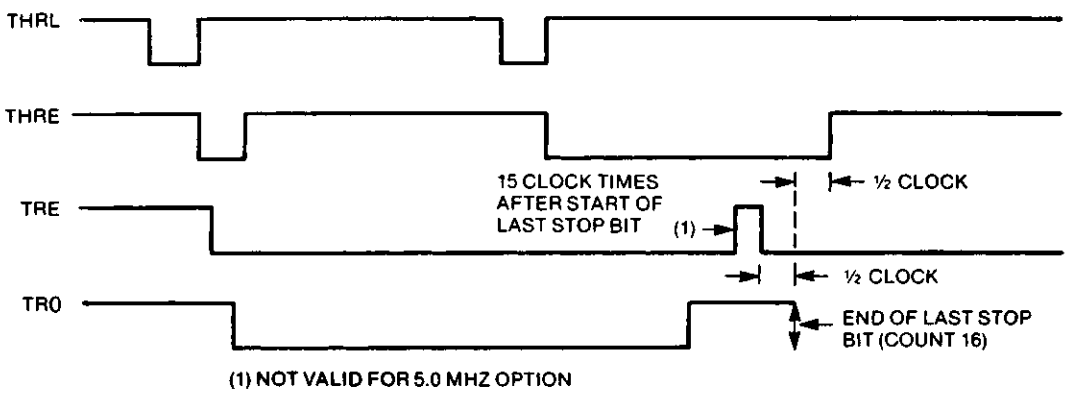
PIN NUMBER	NAME	SYMBOL	FUNCTION
1	POWER SUPPLY	V_{CC}	+5 volts supply
2	NC	NC	No Internal Connection
3	GROUND	V_{SS}	Ground = 0V
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_{1-8} data outputs (pins 5-12).
5-12	RECEIVER HOLDING REGISTER DATA	RR_8-RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	PARITY ERROR	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity differ from that which is programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FRAMING ERROR	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register, FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).

PIN DEFINITIONS

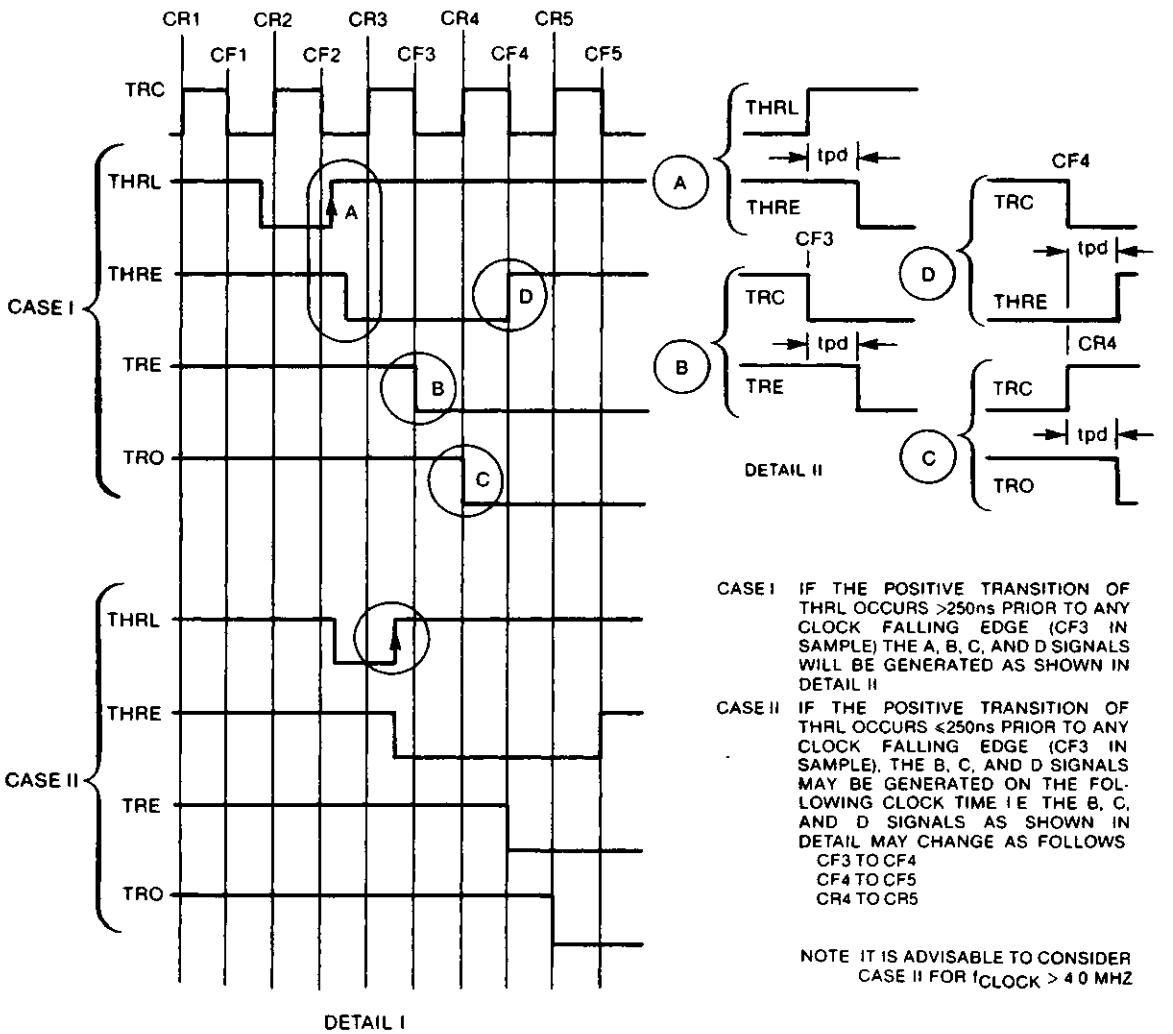
PIN NUMBER	NAME	SYMBOL	FUNCTION
15	OVERRUN ERROR	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	RECEIVER REGISTER CLOCK	RRC	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	DATA RECEIVED RESET	$\overline{DRR}$	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the TRANSMITTER and RECEIVER HOLDING REGISTERS, the TRANSMITTER REGISTER, FE, OE, PE, DR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD	$\overline{THRL}$	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage V_{OH}, to a low-level output voltage V_{OL}.
26-33	TRANSMITTER REGISTER DATA INPUTS	TR_1-TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, TR_1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited, the STOP bit(s) will immediately follow the last data bit of transmission.
36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. The TR1863 and TR1865 generate 1½ stop bits when word length is 5 bits and SBS is High V_{IH}.
37-38	WORD LENGTH SELECT	WLS_2-WLS_1	These two lines select the character length (exclusive of parity) as follows: WLS_2 / WLS_1 / Word Length V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EVEN PARITY ENABLE	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRANSMITTER REGISTER	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.



(1) NOT VALID FOR 5.0 MHZ OPTION

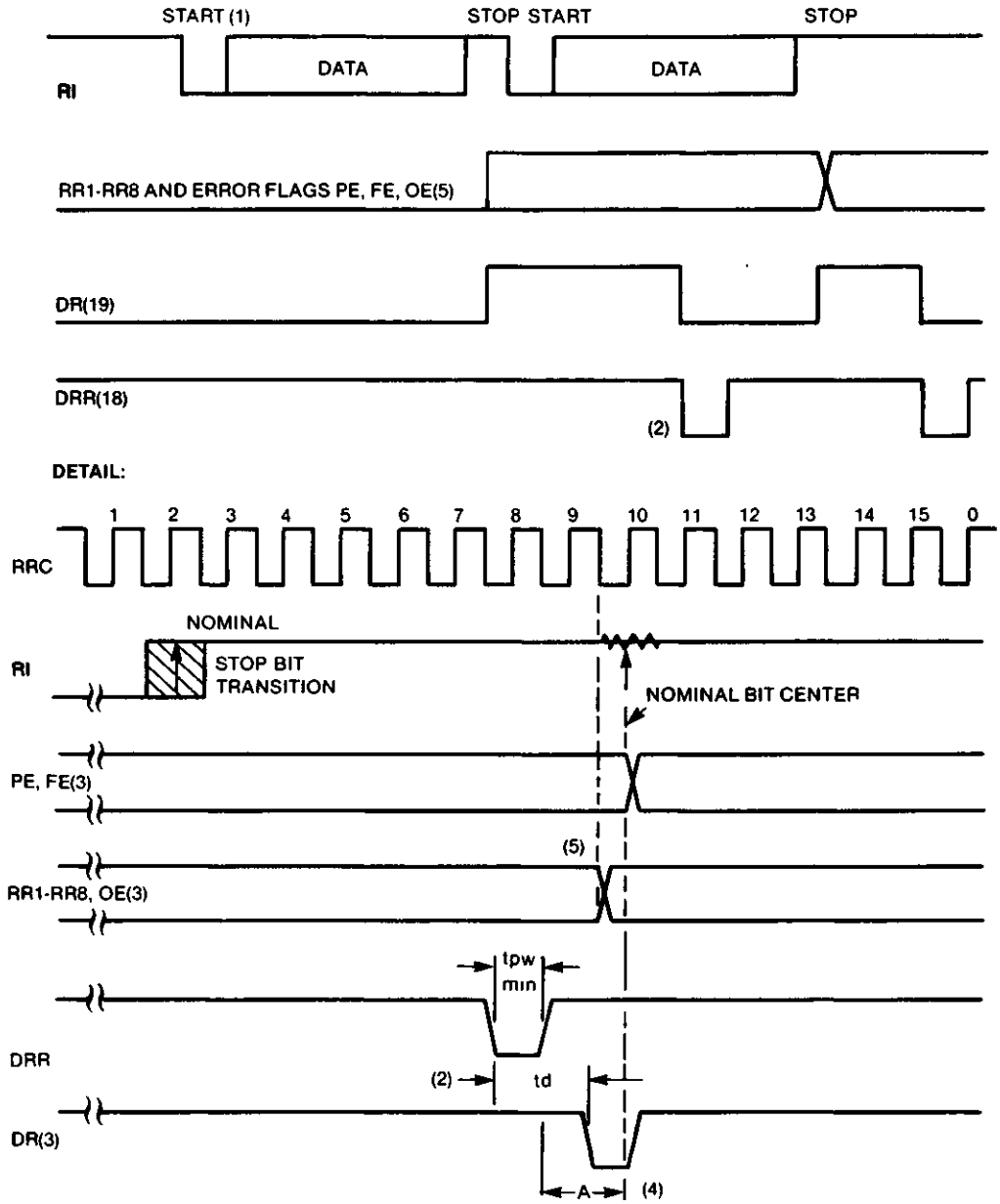


CASE I IF THE POSITIVE TRANSITION OF THRL OCCURS >250ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE) THE A, B, C, AND D SIGNALS WILL BE GENERATED AS SHOWN IN DETAIL II

CASE II IF THE POSITIVE TRANSITION OF THRL OCCURS ≤250ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE), THE B, C, AND D SIGNALS MAY BE GENERATED ON THE FOLLOWING CLOCK TIME I E THE B, C, AND D SIGNALS AS SHOWN IN DETAIL MAY CHANGE AS FOLLOWS
CF3 TO CF4
CF4 TO CF5
CR4 TO CR5

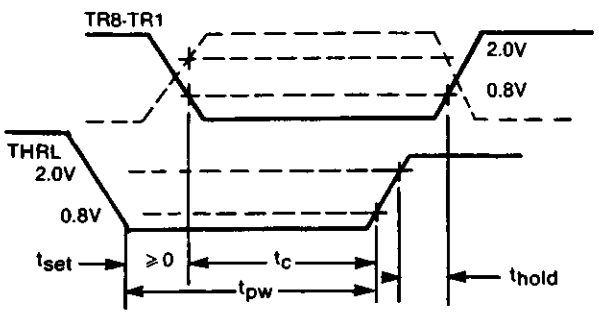
NOTE IT IS ADVISABLE TO CONSIDER CASE II FOR f_{CLOCK} > 4 0 MHZ

TRANSMITTER TIMING

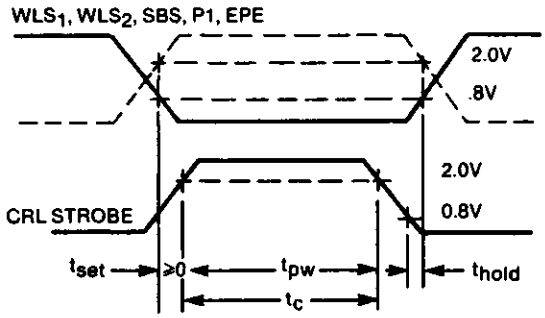


(1) SEE APPLICATION FLAGS REPORT NO. 1 FOR DESCRIPTION OF START BIT DETECTION
(2) THE DELAY BETWEEN DRR AND DR = td = 500 NS
(3) DR. ERROR FLAGS, AND DATA ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT
(4) DRR SHOULD BE HIGH A MINIMUM OF "A" NS (ONE-HALF CLOCK TIME PLUS tpd) PRIOR TO THE RISING EDGE OF DR
(5) DATA AND OE PRECEDES DR, PE, AND FE FLAGS BY ½ CLOCK
(6) DATA FLAGS WILL REMAIN SET UNTIL A GOOD CHARACTER IS RECEIVED OR MASTER RESET IS APPLIED.

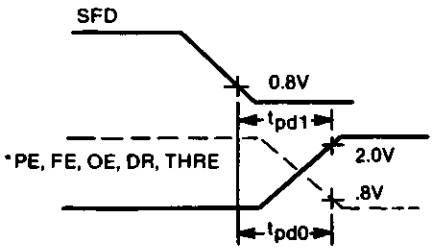
RECEIVER TIMING



DATA INPUT LOAD CYCLE

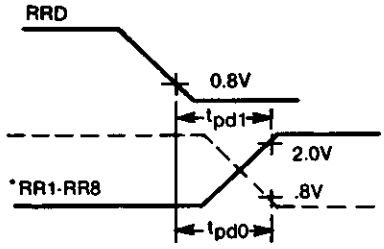


CONTROL REGISTER LOAD CYCLE



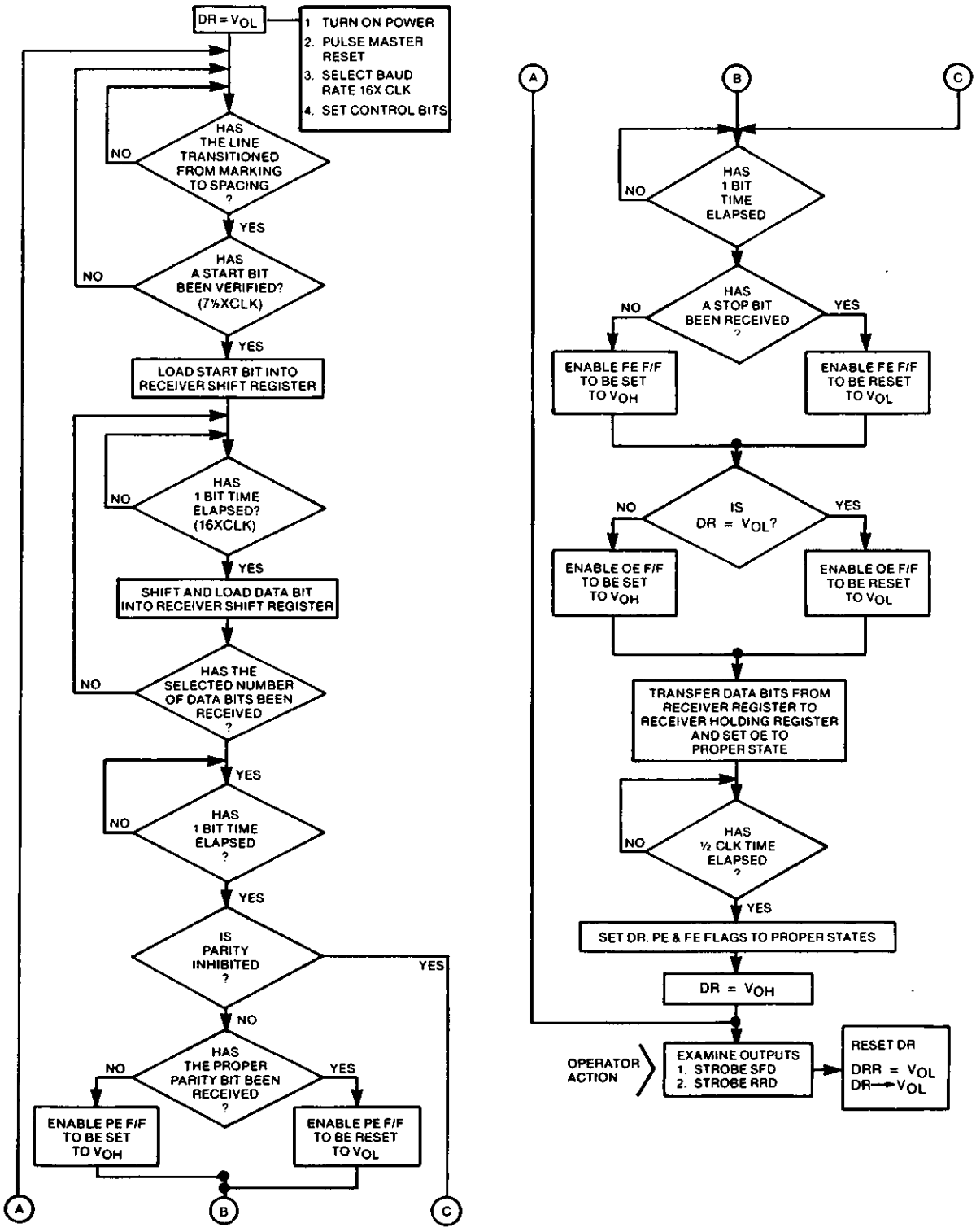
*OUTPUTS PE, FE, OE, DR, THRE ARE DISCONNECTED AT TRANSITION OF SFD FROM 0.8V TO 2.0V.

STATUS FLAG OUTPUT DELAYS

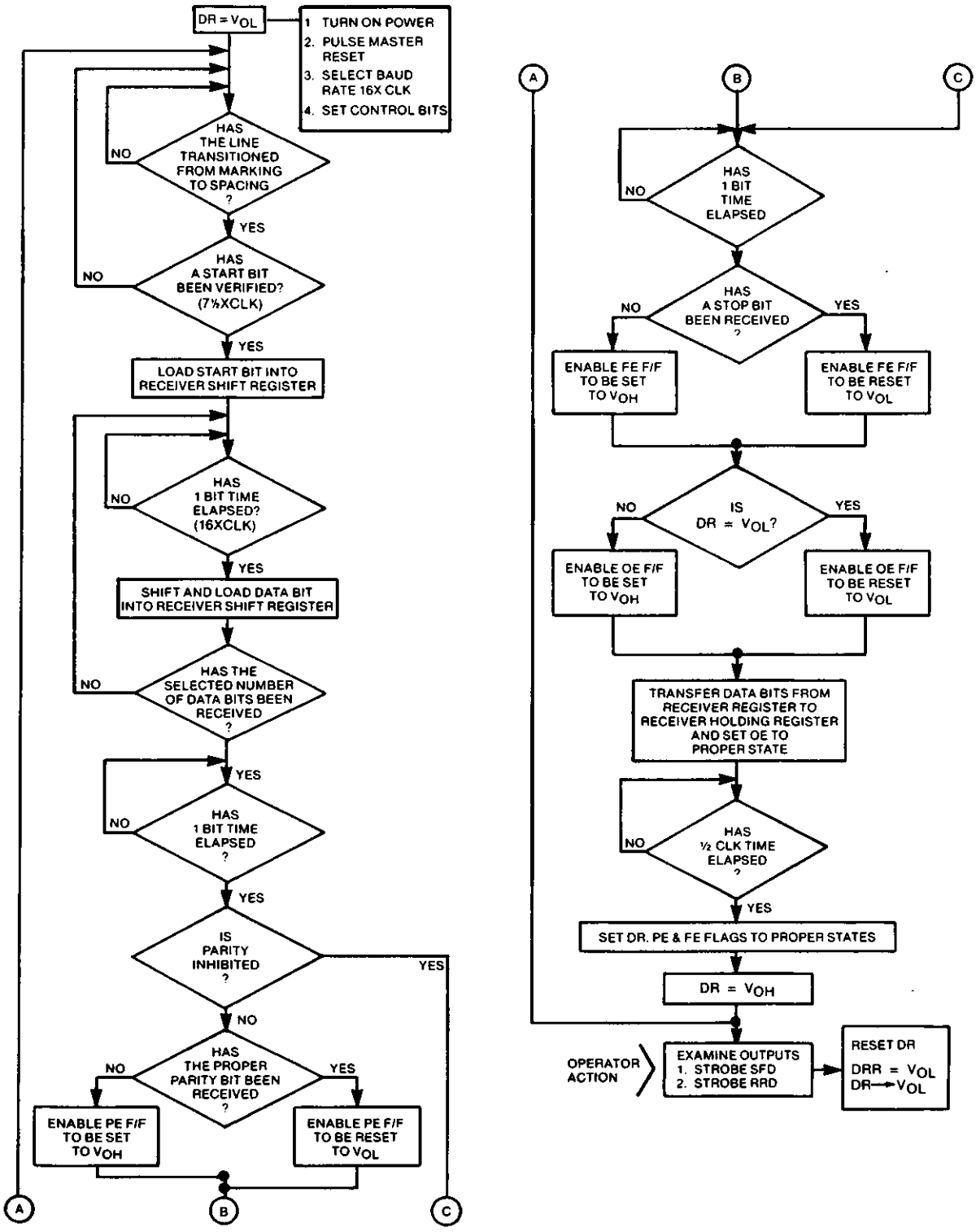


*RR_1-RR_3, ARE DISCONNECTED AT TRANSITION OF RRD FROM 0.8V TO 2.0V.

DATA OUTPUT DELAYS



RECEIVER FLOW CHART



RECEIVER FLOW CHART

ABSOLUTE MAXIMUM RATINGS

NOTE: These voltages are measured with respect to GND

Storage Temperature
  Plastic ..... −55°C to +125°C
  Ceramic ..... −65°C to +150°C
V_{CC} Supply Voltage ..... −0.3V to +7.0V
Input Voltage at any pin ..... −0.3V to +7.0V
Operating Free-Air Temperature
  T_A Range ..... 0°C to 70°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 5%, V_{SS} = 0V)

SYMBOL	PARAMETER	TR1863/5		
	OPERATING CURRENT	MIN	MAX	CONDITIONS
I_{CC}	Supply Current		35ma	V_{CC} = 5.25V
	LOGIC LEVELS			
V_{IH}	Logic High	2.4V		
V_{IL}	Logic Low		0.6V	V_{CC} = 4.75V
	OUTPUT LOGIC LEVELS			
V_{OH}	Logic High	2.4V		V_{CC} = 4.75V, I_{OH} = 100 μa
V_{OL}	Logic Low		0.4V	V_{CC} = 5.25V, I_{OL} = 1.6 ma
I_{OC}	Output Leakage (High Impedance State)		± 10μa	V_{OUT} = 0V, V_{OUT} = 5V SFD = RRD = V_1H
I_{IL}	Low Level Input Current	100μa	1.6ma	V_{IN} = 0.4V TR 1865 only
			10μa	V_{IN} = V_{IL}, TR 1863 only
I_{IH}	High Level Input Current		− 10μa	V_{IN} = V_{IH}, TR 1863 only

SWITCHING CHARACTERISTICS
(See "Switching Waveforms")

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
f_{clock}	Clock Frequency			V_{CC} = 4.75V
	TR1863-00	DC	1.0 MHz	
	TR1863-02	DC	2.5 MHz	
	TR1863-04	DC	3.5 MHz	
	TR1863-06	DC	5.0 MHz	
	TR1865-00	DC	1.0 MHz	with internal pull-ups on all inputs
	TR1865-02	DC	2.5 MHz	with internal pull-ups on all inputs
	TR1865-04	DC	3.5 MHz	with internal pull-ups on all inputs
	TR1865-06	DC	5.0 MHz	with internal pull-ups on all inputs
t_{pw}	Pulse Widths			
	CRL	200 ns		
	THRL	200 ns		
	DRR	200 ns		
	MR	500 ns		
t_c	Coincidence Time	200 ns		
t_{hold}	Hold Time	20 ns		
t_{set}	Set Time	0		
	OUTPUT PROPAGATION DELAYS			
t_{pd0}	To Low State		250 ns	
t_{pd1}	To High State		250 ns	C_L = 20 pf, plus one TTL load
	CAPACITANCE			
c_{in}	Inputs		20 pf	f = 1 MHz, V_{IN} = 5V
c_o	Outputs		20 pf	f = 1 MHz, V_{IN} = 5V

See page 725 for ordering information.

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